Development of Application- Specific Integrated Circuits for Multi-modal, Closed-Loop Neural Prosthetic Devices

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Abstract of "Development of Application- Specific Integrated Circuits for Multi-modal, Closed-Loop Neural Prosthetic Devices", by Farah L Laiwalla, M.D. Ph.D. Brown University, May 2017

Neural Prosthetics are devices that are able to record brain activity and use it to manipulate the environment in a meaningful way. These devices have immense potential for use in patients suffering from neurological illnesses or injuries that have disrupted normal neural pathways. The success of a neural prosthetic device critically relies on the availability of robust long-term access to the brain. This is achieved through a combination of biocompatible sensing probes and integrated electronics platforms. This dissertation addresses the latter by describing the design and testing of custom integrated circuits (ASICs) in three important arenas of implantable, wireless closed-loop neuroprosthetics. Iterative design of a multichannel, low-noise, low-power neural recording amplifier is described in the first part of this work, with special focus on the considerations for migration of the design initially implemented in AMI 1.5µm 1P2M CMOS process to ON-Semi 0.5µm 2P3M CMOS process. The second part of this work focuses on an ASIC approach for long-term interrogation of chronic implants through impedance spectroscopy. Implementation of an ASIC design utilizing a user-programmable on-chip AC voltage source (operating in 1Hz- ~10 kHz range) with individual channel addressability is described, and wideband Impedance Spectroscopy data from benchtop, in-vitro and in vivo characterizations and validation are discussed. The final section of this thesis addresses the development of a closed-loop (bidirectional) neural prosthesis, focusing on the design of an 8-bit current-steering digital to analog

converter (DAC) for patterned Intracortical microstimulation. Simulation and benchtop test data is described, with particular focus on challenges to in-vivo translation.

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Nurmikko AV, Yin M, Patterson WR, Aceros J, Borton DA, **Laiwalla FL**. "Implantable wireless neural device." U.S. Patent Application 14/028,178, filed September 16, 2013.

Nurmikko AV, Donoghue JP, Hochberg LR, Patterson WR, Song YK, Bull CW, Borton DA, **Laiwalla, F**, Park S, Yin M, Aceros J. Listening to brain microcircuits for interfacing with external world—progress in wireless implantable microelectronic neuroengineering devices. *Proceedings of the IEEE.* 2010;98(3):375-88.

Song YK, Borton D, Park S, Patterson W, Bull C, **Laiwalla F**, Mislow, J, Simeral, JD, Donoghue, JP, Nurmikko, AV. Active microelectronic neurosensor arrays for implantable brain communication interfaces. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*. 2009;17(4):339-45.

Zhang J, **Laiwalla F**, Kim JA, Urabe H, Van Wagenen R, Song YK, Connors B, Nurmikko AV. Integrated device for optical stimulation and spatiotemporal electrical recording of neural activity in light-sensitized brain tissue. *Journal of neural engineering*, 2009:(6:05)5007 (Invited paper).

Patterson W., Song Y., Bull C., **Laiwalla F**., Nurmikko A., Donoghue J. CMOS ICs for Brain Implantable Neural Recording Microsystems. Book Chapter in *"CMOS Biotechnology"*. Springer US, 2007.

Jay SM, Skokos E, **Laiwalla F**, Krady MM, Kyriakides TR. Stem Cells, Tissue Engineering and Hematopoietic Elements-Foreign Body Giant Cell Formation Is Preceded by Lamellipodia Formation and Can Be Attenuated by Inhibition of Rac1 Activation. *American Journal of Pathology*. 2007;171(2):632-40.

Laiwalla F, Klemic KG, Sigworth FJ, Culurciello E. An integrated patch-clamp amplifier in silicon-on-sapphire CMOS. *IEEE Transactions on Circuits and Systems,*2006. 53(11):2364-70

ABSTRACTS, POSTERS AND PRESENTATIONS

Zhang J, **Laiwalla F**, Kim J, Van Wagenen R, Song YK, Connors B,Nurmikko AV. Optical Control of Neural Activity by Waveguide Delivery in Genetically Targeted Brain Tissue. *Annual conference of the Optical Society of America, 2009.*

Zhang J, **Laiwalla F**, Kim JA, Urabe H, Van Wagenen R, Song YK, Connors B, Nurmikko AV. A microelectrode array incorporating an optical waveguide device for stimulation and spatiotemporal electrical recording of neural activity. *IEEE Engineering in Biology and Medicine Society Annual Conference*, 2009: 2046-2049.

Borton DA, Song YK, Patterson WR, Bull C, Park S, **Laiwalla F**, Donoghue JP, Nurmikko AV. Wireless, high-bandwidth recordings from non-human primate motor cortex using a scalable 16-Ch implantable microsystem. *IEEE Engineering in Medicine and Biology Society Annual Conference,* 2009: 5531-5534.

Borton D, Song YK, Patterson W, Bull C, Park S, **Laiwalla F**, Donoghue JP, Nurmikko AV. Implantable wireless cortical recording device for primates. *World Congress on Medical Physics and Biomedical Engineering*, 2009:588-91.

Wang J, Zhang J, Borton D, **Laiwalla F**, Burwell R, Nurmikko AV. Integrated device for focal optical stimulation and spatiotemporal electrical recording of neural activity for *in vivo* application. *Annual meeting of the Society for Neuroscience, 2009.*

Laiwalla F, Zhang J, Kim J, Connors B, Song YK, Nurmikko AV "Two-dimensional spatial mapping of epileptic wave propagation using focal stimulation in ex-vivo rodent models", *J. Investigative Medicine*, 2009: **57**(3), 543.

Zhang J, **Laiwalla F**, Kim J, Connors B, Song YK, Nurmikko AV. A dual optical/electrical stimulation and recording probe for high spatiotemporal resolution studies of neural microcircuits. *Annual meeting of the Society for Neuroscience, 2008.*

Laiwalla F, Kim JS, Zhang J, Song YK, Connors B, Nurmikko AV. A multielectrode array platform for high-throughput spatiotemporal mapping in in-vitro neural populations. *Annual meeting of the Society for Neuroscience*, 2008.

Culurciello E, **Laiwalla F**, Fu Z, Klemic K, Sigworth F. An integrated silicon-on-sapphire patch-clamp amplifier. *IEEE/NLM life science systems and application workshop, IEEE*. 2006.

Laiwalla F, Culurciello E., Klemic K., Sigworth F. An integrated Patch Clamp Amplifier in Silicon on Saphhire CMOS. *IEEE International Symposium on Circuits and Systems 2006.*

Laiwalla F, Culurciello E., Klemic K., Sigworth F. Performance analysis of an integrated Patch Clamp Amplifier in Silicon-on-Sapphire CMOS technology. *Connecticut Microelectronic and Optoelectronics Consortium,* 2005.

Laiwalla F, Culurciello E., Klemic K., Sigworth F. Design and Testing of an integrated CMOS Patch Clamp Amplifier. *Connecticut Microelectronic and Optoelectronics Consortium,* 2004.

Xanthopoulos J, **Laiwalla F**, and Majumdar S. Growth Inhibitory Response of Mouse Mammary Carcinoma Cells to Anastrazole. *Journal of the Pennsylvania Academy of Science.* 76 (2003): 142.

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Chapter 1: Introduction

It has taken over two billion years of evolution to produce the masterpiece that is the brain. It is postulated that this journey began when single-celled sponges figured out the basic electrochemical mechanism of inter-organism communication. Today, the 100 billion neurons in the brain work in organized groups with multi-tiered, modulated feedback to sense stimuli, move muscles, perceive abstractions, form and manipulate memories and create the unique output that we call the human experience. That the brain motivates scientists to understand it and inspires engineers to emulate it is inevitable, and the field of brain-computer interfaces (BCI) is the culmination of these joint aspirations.

Myriad approaches have been applied through history to study the brain [1], but it was the invention of the electroencephalogram (EEG) by Hans Berger in 1929 [2] that was ultimately instrumental in enabling organized study of neural circuits. Single-operant conditioning experiments by Fetz and Kamiya [3] further demonstrated that neural modulation could be learned, thus setting the basis of BCI methodology. Niels Birbaumer subsequently trained paralyzed people to self-regulate slow cortical potentials in EEG to control a cursor [3], demonstrating the first successful BCI. The recent development of high-density electrode arrays, microelectronic recording platforms and computational decoding techniques has provided significant impetus to the field, which has evolved into a multidisciplinary

hub of ideas from neuroscience, computer science and several branches of engineering. There are a few rudimentary principles, however, that have continued to persist and are outlined below.

1.1 Brain-Computer Interfaces: Definitions and Descriptions

The First International meeting of Brain-Computer Interface (BCI) Technology took place in 2000. This alludes to the relatively young nature of the field, yet one of the topics of extensive discussion during this meeting was the difficulty in comparing BCI literature due to the lack of standardization of terminology and protocols in the field [3,4]. This is perhaps a necessary evil of a field that has drawn researchers from so many different disciplines; it also makes it pertinent and important to start this section by defining the specific wordage used in this thesis.

- **Brain-Computer Interface**: A communication system that does not rely on the brain's normal output pathways of peripheral nerves and muscles. Used interchangeably with **Neuro or Neural Prosthesis**. This includes both afferent and efferent communication with the nervous system.
- **Neural Sensor:** the physical interface with neural tissue, which typically constitutes a microelectronic device for transduction of neural activity and packaging it for transmission to the computer.
- **Decoder:** Decoding is the task of determining the neural population dynamics through algorithmic processing on a computer.

- **Effector or Actuator**: Devices such as robotic arms, motorized wheelchairs, computer cursors or nerve-cuff-electrodes which may be driven by "decoded" neural data, where the latter is obtained as described above.

A sensor, decoder and effector constitute an efferent Neuroprosthetic system, as demonstrated in Figure 1.1.

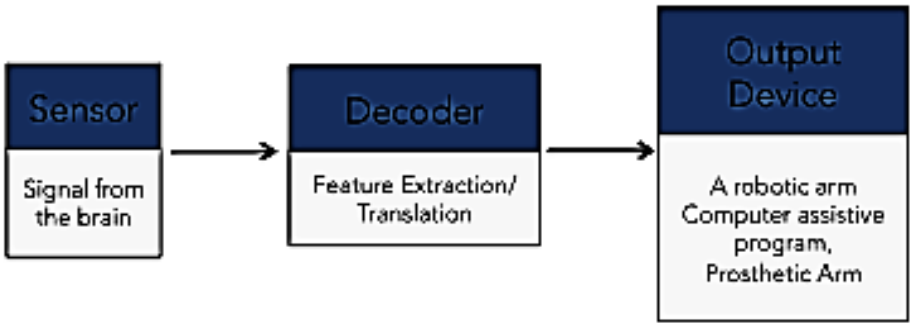


Figure 1.1: Building Blocks of a Neural Prosthesis

Experimental methodology is a crucial factor driving the demands on a neuroprosthetic device. Two common concepts in motor neuroprosthetics research are:

- **Cursor-Control paradigm**: this is a commonly used experimental paradigm in motor neuroprosthetics research [5, 6, 13], including the BrainGate™ clinical trial which this research is anticipated to merge with. It relies on motor cortical neural output to control a computer cursor, as show in Figure 1.2.
- **Closed-loop control:** this refers to the ultimate goal in BCI research to utilize both afferent and efferent neural pathways through a combination of neural recording and patterned microstimulation. The work described in Chapter 5 forays

into this arena. It may also describe the closed-loop formed through visual or other sensory feedback.

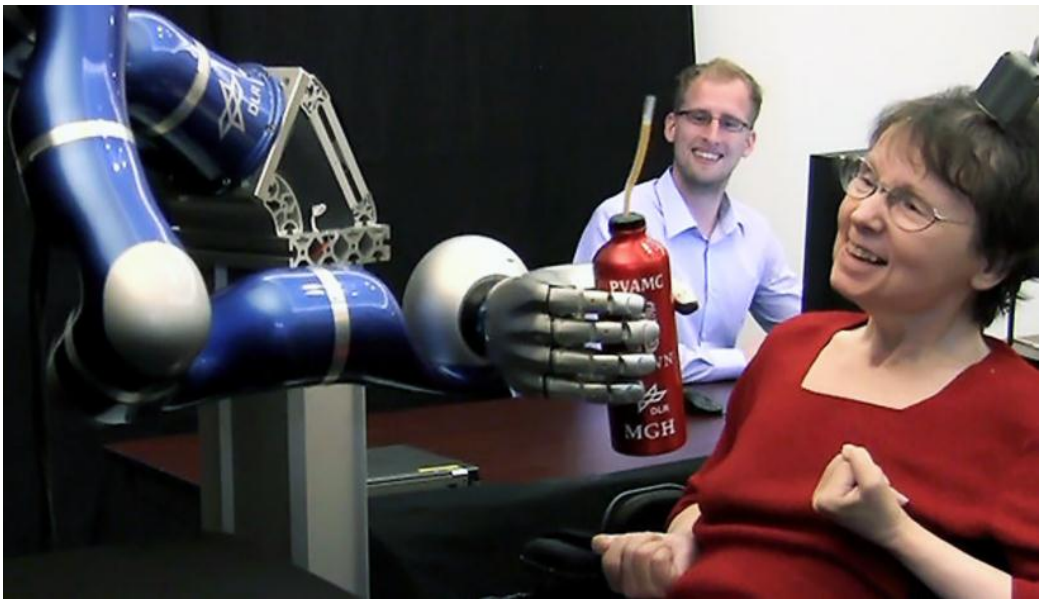


Figure 1.2: A Brain gate subject using spike-activity from motor cortex (M1) to manipulate a robotic arm carrying a water bottle to the appropriate position for the subject to drink from it [7].

The properties of the physical device and the duration of implantation determine several engineering design considerations. As such, implants are described in the following terms:

- **Passive Implant:** Functionality relies on the material properties alone. Does not usually need constant invasive monitoring, and degradation is related to material wear down. Isolated multi-electrode arrays and wire implants are examples of passive implants
- **Active Implant:** Senses and/or modulation of physiologic activity continually. This requires integrated electronics, and thus poses challenges in power delivery, hermetic sealing [8-10], tissue heating and telemetry [11, 12]. Many modern

implants (cardiac, drug delivery etc) fall in this category, as do the devices that this work is contributing to.

- **Acute/Sub-acute Implant**: This refers to implant duration. An acute implant refers to a short time period from minutes to hours (as in an intra-operative implant). The term "sub-acute" is reserved for short-term implants lasting up to 30 days.

- **Chronic Implant:** An implant designed to last for months to years (the constraints of device longevity are typically battery life; acceptable degradation rate for other components is on the order of decades). Designs described in this work are aimed for chronic implants.

Chronic Neural implants exploit certain features of Brain anatomy to facilitate meeting the specifications for active biomedical implants. Figure 2.3 shows a cross-section diagram of the brain, and the various pertinent structures are discussed below.

- **The Dura and Subdural Space***:* Dura mater is the outermost meningeal covering of the brain. Neural sensor probes traverse this layer, resting in the **subdural space** (for planar electrodes) and penetrating into Cortex (for Penetrating electrodes). A good post-implant dural seal is important for minimization of infection risk. Additionally, shear forces on the dura can lead to intracranial hemorrhages [10,11] and should be carefully mitigated. The sub-dural space, also referred to as "Epicortical space", contains Cerebro-spinal Fluid (CSF) and acts to distributes load-forces through this fluid [13,14].

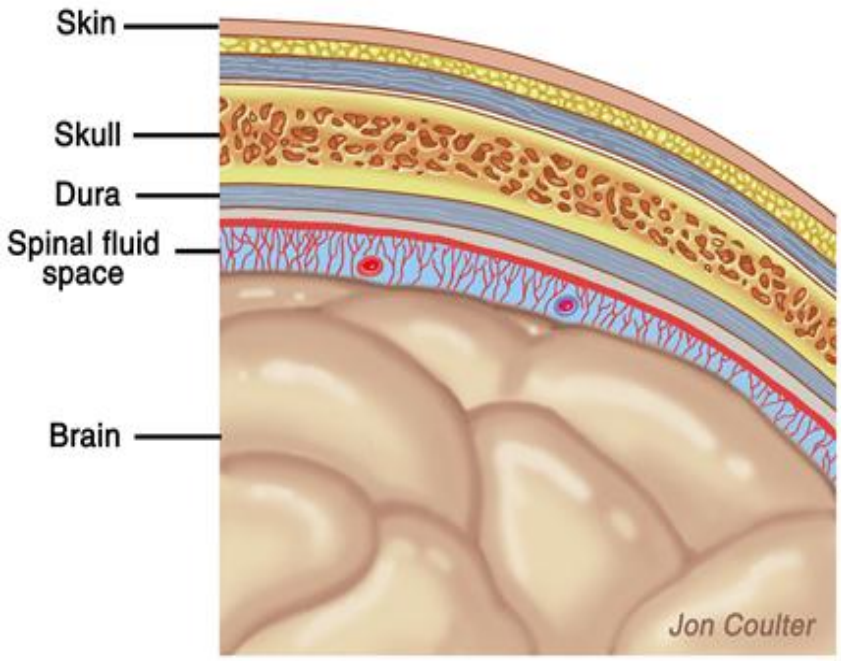


Figure 1.3: Diagrammatic representation of the anatomy of intracranial, extra-cortical space.

- **Cranium (skull) and the Epi-cranial space**: The skull serves as a rigid boundary for intracranial contents, and is usually also utilized for affixing the implant. An avascular structure with thickness ranging from 3-11 mm [15], it may at times be thinned to create an implant seating cavity. The potential space between the rigid skull and the flexible overlying skin is termed the epi-cranial space. Much of the implant bulk resides here, because skin provides easy access for both **percutaneous** (wires through skin) and **transcutaneous** (wireless optical or RF) telemetry. The high vascularization of skin is also helpful for implant heat dissipation.

1.2 Types of Neural Signals and Recording Electrodes

All Cortical Neural signals can ultimately be traced by to cellular Action Potentials [16], and are thus defined in relation to their distance from the signal source (and hence their degree of spatial and temporal summation) [17-19]. Recording electrode geometry plays a critical role in defining spatial summation limits as summarized in Figure 1.2. Electrodes are either classified as planar (disc) or penetrating; biocompatible high-conductivity metals are the material of choice for both, and the latter may also avail microelectronics approaches for creating dense, integrated structures (such as the Utah MicroElectrode Array).

Planar electrodes are widely used in research and clinical neuroscience (EEG and ECoG). A single EEG electrode performs volume summation over $6cm^3$ of cortex. Multichannel systems with overlapping "receptive fields" yield characteristic low frequency rhythms, referred to as EEG bands, (shown in Figure 1.3). Even though the bandwidth of EEG activity is < 50 Hz, self-regulation for control of BCIs has been demonstrated in several bands [20-23].

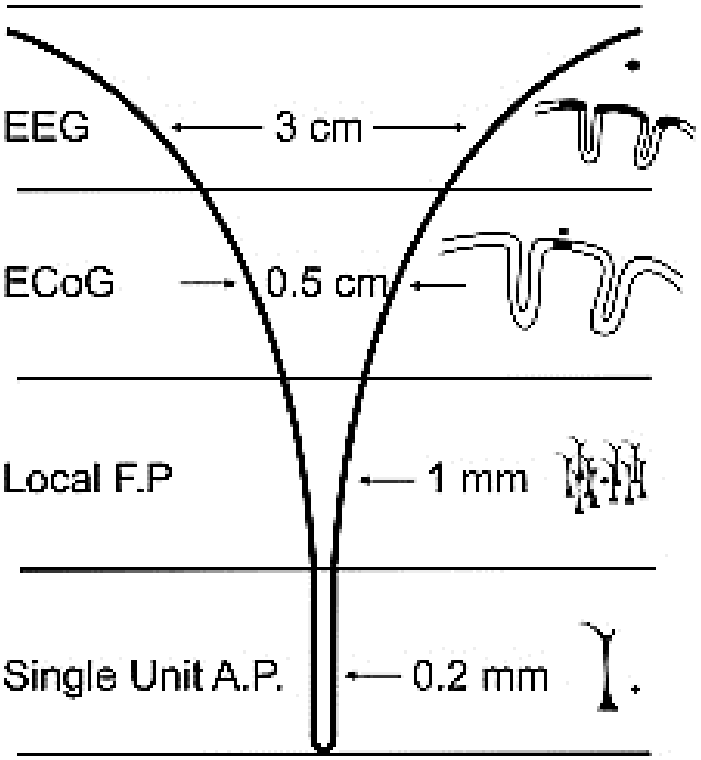


Figure 1.4: Spatial scales associated with different types of Neural Signals. From [28].

ECoG electrodes operate on the same principles as EEG, but their smaller size, tighter pitch and placement location (surgical implant in the subdural space) affords then gains in both temporal and spatial resolution. Developed by Penfield predominantly used for seizure-focus localization, ECoG offer signal bandwidth up to 500 Hz [22], and is becoming increasingly popular for BCI applications [24-26].

Penetrating electrodes may either be integrated microelectrode arrays or microwires. The latter can use a variety of materials, but stainless steel, Pt-Ir, IrOx or Tungsten are the most popular. The tapered geometry enhances both proximity to the source as well as probe focality [27]. The obvious downside is invasiveness, and these probes have also been implicated in tissue inflammation due to brain micromotion-associated shear forces. Figure 1.6 shows the major types of penetrating electrodes used in BCIs.

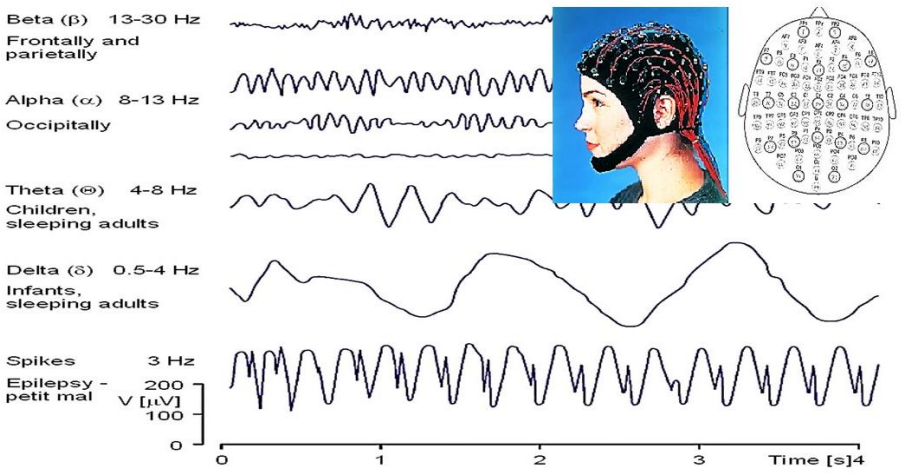


Figure 1.5: EEG bands. Alpha waves are associated with awake relaxation with closed eyes, Rhythmic "spikes" are characteristic of seizures.

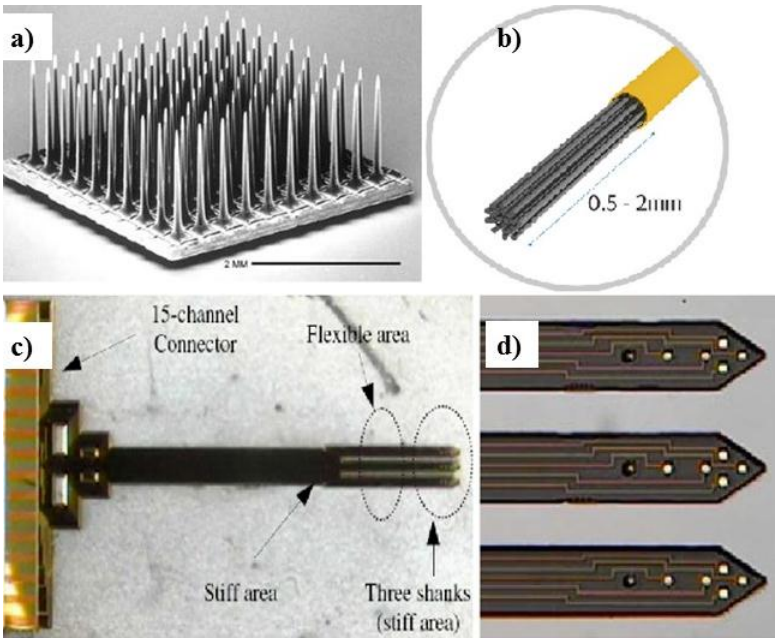


Figure 1.6: Types of Penetrating Electrodes. (a) Utah Microelectrode array, comprising micromachined silicon with Platinum tips.(b) Platinum- Iridium Microwires. (c and d) Michigan Probe with planar silicon shanks, each with multiple metal contacts.

The types of signals obtained through these probes are classified according to the signal's frequency content. Low frequency signals (up to 250 Hz) are termed **Field Potentials** (including **Local Field Potentials** obtained through penetrating

electrodes) while high-frequency signals (> 500 Hz) are called **Spikes** (which could represent S**ingle-Unit Activity (SUA)** or **Multi-Unit Activity (MUA)).** The latter have the most information content, and are the signals of choice for BCI decoders [28,29]. The term "**broadband**" in this context contains both field potentials and spikes, and is in the mHz- 5 kHz range.

1.3 Configurations for Wireless Implantable Neural Recording Systems

This work describes the development of integrated electronics to be used in Wireless Implantable Neuroprosthetics. A brief overview of the platform technologies this research is targeted for is provided here, with references to particular subsystem components that were designed during this research.

Three different but related topologies for implantable recording systems have been developed by our group in the last decade [28-32]. Figure 1.7 provides the shared block diagram of the components of each of these recording systems. Specifications and constraints for each sub-component were developed in accordance with biomedical implant regulatory guidelines (A formal document created for purposes of technology translation is included as Appendix IA).

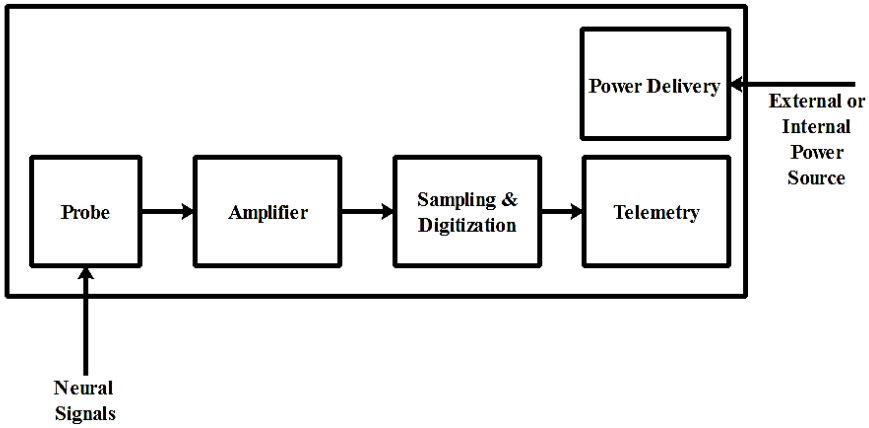


Figure 1.7: A block diagram of the electronic components of a Neural Recording System

- ***Polymer-Encapsulated "Brain- Implantable Chip" :*** This system uses inductive coupling for power delivery and utilizes optical transcutaneous telemetry (Vertical Cavity laser at 800 nm) . Redesign of the clock extraction circuitry (from RF carrier signal) and laser driver were completed during this research and are described in [28] and revisited in Chapter 2. Figure 1.8 demonstrate the two variants of this system: a single ADC 16-channel system [29, 30] and a dual-front-end system supporting 2 ADCs each with a separate electrode array [31]. Development of the latter required redesign of the data-handling Digital Controller Chip, also addressed in Chapter 2.

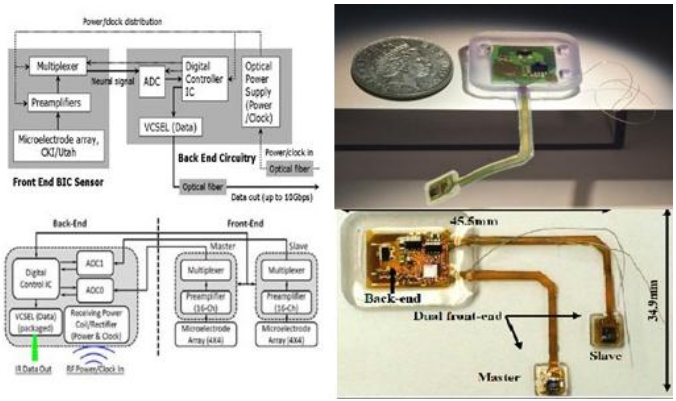


Figure 1.8: Polymer-encapsulated RF-powered BIC systems with optical telemetry.

An important feature of the BIC systems was the direct integration of amplifier ASICs with the Utah MEA [29]. The 16-channel amplifier ASIC (shown in Figure 1.9) was expressly designed for this integration; redesign of this ASIC with CMOS process migration and participation in the subsequent scaling of the design from 16 to 100 channels is one of the major contributions of this work.

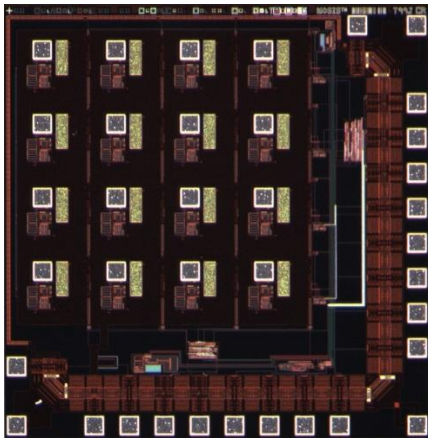


Figure 1.9: Photomicrograph of the 16-channel amplifier ASIC

- ***Full-Implantable, Battery-Powered, Hermetically-Sealed***

"Subcutaneous Brown Neuro-Card System (SBNC)": This system features a rechargeable battery and active electronics in a Titanium enclosure placed in the epi-cranial space. A passive microelectrode array is coupled through 100-feedthroughs in the Ti casing. A sapphire window provides RF transparency for battery recharge and data telemetry (RF) as shown in Figure 1.10. This is the primary platform that all IC development work described in this thesis is directly aimed for. The early development of this architecture was part of my research as has been the clinical translation of this device.

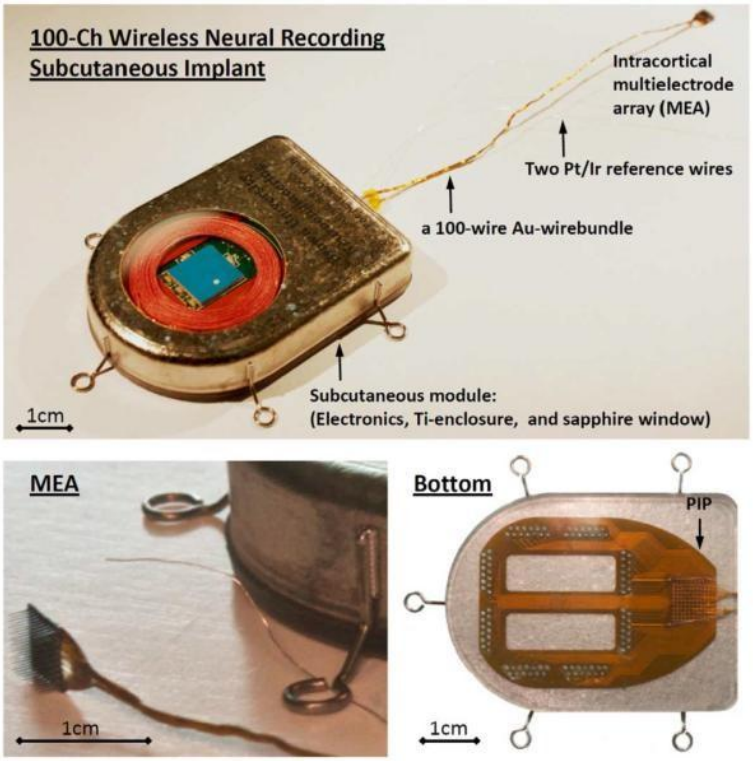


Figure 1.10: The fully implantable hermetically sealed wireless Neural Recording System. A passive Utah MEA is attached through a gold-wire bundle (Bottom Left) through ceramic feedthroughs (Bottom Right). From [32].

- ***External, Battery-Powered Wireless Neural Recording Systems with Custom RF Transmitter:*** This battery-powered head-mounted system (shown in Figure 1.11) is electronically identical to the SBNC with the exception of a custom RF ASIC (not part of this work, described in [33]). It is primarily targeted for research with free- moving animals, but also offers the capability to tap into the entire animal and human subject population with percutaneous Utah MEAs. The system design for this platform is utilized in testing the novel ASIC described in Chapters 3 and 4 of this work.

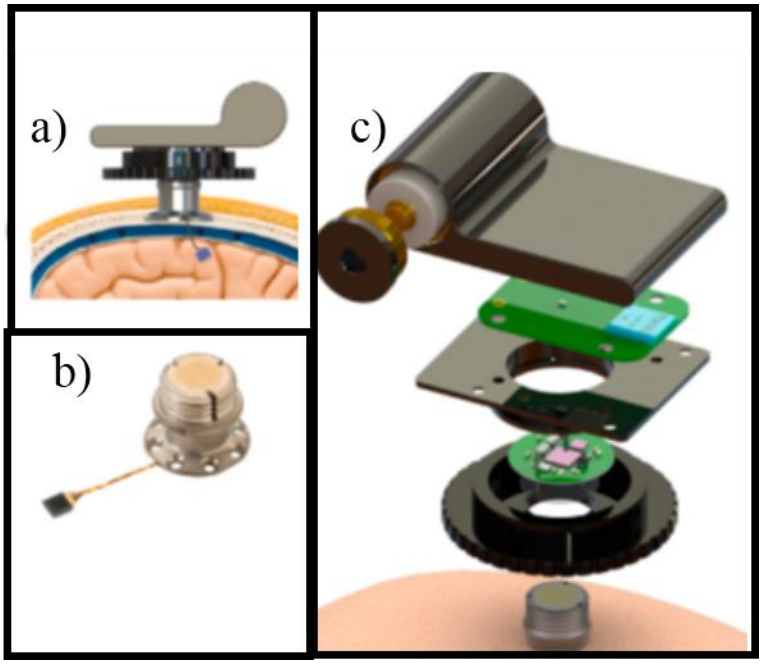


Figure 1.11 (a) (Left Top): An external head-mounted, battery powered, wireless neural recording system. (b) (Left Bottom) Passive Utah Electrode Array that the system mates with. (c) (Right) An exploded view of the system showing various components. From [33].

1.4 Organization of this Dissertation

The rest of this document is organized as follows: Chapter 2 delves into the details of custom ASIC design for a broad-band, wireless neural recording platform, and identifies specific contributions made to the design of analog neural recording amplifiers as part of this work. Chapters 3, 4 and 5 discuss the major novel contributions of this work to the project at large. Chapter 3 introduces the concept of long-term monitoring of the tissue-electrode interface through use of impedance spectroscopy and describes integrated circuit approaches implemented as part of this dissertation. Chapter 4 focuses on the development and testing of a wired, external recording system incorporating impedance spectroscopy. Chapter 5 describes development of a bidirectional ASIC incorporating recording and programmable patterned microstimulation for closed-loop neural prosthetic applications. Finally,

Chapter 6 discusses current and future directions for novel ASIC development for neural prosthetics. Appendix I identifies contributions made in the realm of data collection, organization and documentation as part of a translational effort for the SBNC device described above. Appendix II provides details of the technology migration process for the amplifier ASIC.

1.5 Specific Contributions

This systems described in this dissertation are the product of a large team of engineers. This section outlines my specific focus and contributions to the group research:

- ***Contributions to ASIC design***

The redesign of the Neural recording amplifier, from technology migration to iterative redesign of various sub-components was been completed by me. This includes transistor level design, simulations and bench top testing. This work is represented in [28] and [30], where I am co-author.

Design, simulation, layout and benchtop as well as in-vivo testing of the impedance spectroscopy ASIC was completed by me, which is the leading contribution of this work. This also involved PCB design and modifications the signal acquisition system. An FPGA-based command delivery system and de-novo signal analysis software were also developed for this purpose. A subset of the bench top characterizations of the ASIC were completed by a collaborator, but the design and specific implementation of the tests were driven by me.

Contributions to the design of the 16-channel microstimulation ASIC were made as part of this work. This included transistor-level design of the current-steering DAC, layout and simulation of the design and bench-top testing described in Chapter 5.

Several ASIC redesign tasks (not included in this dissertation) were completed during this research, including a RF clock-extraction comparator and a low-drop out voltage regulator on digital controller ASIC. VHDL Synthesis, simulations and testing of the redesigned controller ASIC were also completed by me.

- ***Contributions to Systems Level Implementations***

Contributions to early versions of the in-house Neural Data Acquisition system were made by me. Initial work on the implementation of SBNC was spearheaded by me (yielding inventor status in the device patent [34]. This included board-level design and vendor selection for fabrication and packaging. More recently, I have made significant contributions in the translation effort (in the realm of ASIC design and documentation), as described in Appendices I A-C.

1.6 References

1. Afifi, A.K. and Bergman, R.A., Functional Neuroanatomy, New York: McGraw-Hill, 1998. The margins of this text are filled with historical facts about the origins of neuroanatomical structures and discoveries.

2. Collura, Thomas F. "History and evolution of electroencephalographic instruments and techniques." Journal of clinical neurophysiology 10, no. 4 (1993): 476-504.

3. Birbaumer, Niels, and Leonardo G. Cohen. "Brain–computer interfaces: communication and restoration of movement in paralysis." The Journal of physiology 579, no. 3 (2007): 621-636.

4. Wolpaw, Jonathan R., Niels Birbaumer, William J. Heetderks, Dennis J. McFarland, P. Hunter Peckham, Gerwin Schalk, Emanuel Donchin, Louis A. Quatrano, Charles J. Robinson, and Theresa M. Vaughan. "Brain-computer interface technology: a review of the first international meeting." IEEE transactions on rehabilitation engineering 8, no. 2 (2000): 164-173.

5. Vidaurre, Carmen, and Benjamin Blankertz. "Towards a cure for BCI illiteracy." Brain topography 23, no. 2 (2010): 194-198.

6. Black, Michael J., Elie Bienenstock, John P. Donoghue, Mijail Serruya, Wei Wu, and Yun Gao. "Connecting brains with machines: the neural control of 2D cursor movement." In Proc. 1st International IEEE/EMBS Conference on Neural Engineering, pp. 580-583. 2003.

7. Serruya, M., A. Caplan, M. Saleh, D. Morris, and J. Donoghue. "The braingate pilot trial: Building and testing a novel direct neural output for patients with severe motor impairment." In Soc. for Neurosci. Abstr. 2004.

8. Takeuchi ES, Leising, RA. "State of the Art Batteries for Implantable Medical Devices". Accessed March 21st 2016. http://www.electrochem.org

9. Joung, Yeun-Ho. "Development of implantable medical devices: from an engineering perspective." International neurology journal 17, no. 3 (2013): 98-106.

10. Ely, Kevin. Issues in Hermetic Sealing of Medical Products. Accessed April 25th, 2016. http://www.mddionline.com/article/issues-hermetic-sealing-medical-products.

11. Miller, J. A., G. Belanger, I. Song, and F. Johnson. "Transcutaneous optical telemetry system for an implantable electrical ventricular heart assist device." Medical and Biological Engineering and Computing 30, no. 3 (1992): 370-372.

12. Ackermann Jr, D. Michael, Brian Smith, Xiao-Feng Wang, Kevin L. Kilgore, and P. Hunter Peckham. "Designing the optical interface of a transcutaneous optical telemetry link." Biomedical Engineering, IEEE Transactions on 55, no. 4 (2008): 1365-1373.

13. Voorhies, Jason, and Aaron Cohen-Gadol. "Techniques for placement of grid and strip electrodes for intracranial epilepsy surgery monitoring: Pearls and pitfalls." Surgical neurology international 4 (2013): 98.

14. Arya, Ravindra, Francesco T. Mangano, Paul S. Horn, Katherine D. Holland, Douglas F. Rose, and Tracy A. Glauser. "Adverse events related to extra-operative

invasive EEG monitoring with subdural grid electrodes: A systematic review and meta-analysis." Epilepsia 54, no. 5 2013): 828-839.

15. Deloye, Adelola, Kenneth R. Kattan, and Frederic N. Silverman. "Thickness of the normal skull in the American blacks and whites." American Journal of Physical Anthropology 43, no. 1 (1975): 23-30.

16. Shepherd, Gordon. "An Interactive Tutorial." Accessed April 2nd 2016. http://medicine.yale.edu/lab/mccormick/publications/eotn_165502_284_19929.pdf

17. Gumbart, James, Fatemeh Khalili-Araghi, Marcos Sotomayor, and Benoît Roux. "Constant electric field simulations of the membrane potential illustrated with simple systems." Biochimica et Biophysica Acta (BBA)-Biomembranes 1818, no. 2 (2012): 294-302.

18. Tallgren, Pekka, Sampsa Vanhatalo, Kai Kaila, and Juha Voipio. "Evaluation of commercially available electrodes and gels for recording of slow EEG potentials." Clinical Neurophysiology 116, no. 4 (2005): 799-806.

19. Ollikainen, Jorma O., Marko Vauhkonen, Pasi A. Karjalainen, and Jari P. Kaipio. "Effects of electrode properties on EEG measurements and a related inverse problem." Medical engineering & physics 22, no. 8 (2000): 535-545.

20. R. Cooper, A. L. Winter, H. J. Crow, and W. G. Walter, Comparison of subcortical, cortical and scalp activity using chronically indwelling electrodes in man," Electroencephalogr Clin Neurophysiol, vol. 18, pp.217-28, Feb 1965.

21. D. J. McFarland, D. J. Krusienski, W. A. Sarnacki, and J. R. Wolpaw, Emulation of computer mouse control with a noninvasive brain computer interface," J Neural Eng, vol. 5, no. 2, pp. 101-10, Jun 2008.

22. A. Belitski, A. Gretton, C. Magri, Y. Murayama, M. A. Montemurro,N. K. Logothetis, and S. Panzeri, Low-frequency local field potentials and spikes in primary visual cortex convey independent visual information," J Neurosci, vol. 28, no. 22, pp. 5696-709, May 2008.

23. Jonathan Wolpaw, Elizabeth Winter Wolpaw. Brain-Computer Interfaces: Principles and Practice. Chapter 15.

24. Wang, Wei, Jennifer L. Collinger, Alan D. Degenhart, Elizabeth C. Tyler-Kabara, Andrew B. Schwartz, Daniel W. Moran, Douglas J. Weber et al. "An electrocorticographic brain interface in an individual with tetraplegia." PloS one 8, no. 2 (2013): e55344.

25. Schalk, S., McFarland , D., Hinterberger, T., Birbaumer, N., & Wolpaw , J. (2004). Bci2000: A general-purpose brain-computer interface (bci) system . IEEE Transactions on Biomedical Engineering , 51(6), 1034-1043.

26. . Charvet, F. Sauter-Starace, M. Foerster, D. Ratel, C. Chabrol,J. Porcherot, S. Robinet, J. Reverdy, R. D'Errico, C. Mestais, and A. Benabid, Wimagine : 64-channel ecog recording implant for human applications," in Engineering in Medicine and Biology Society (EMBC), 2013 35th Annual International Conference of the IEEE, July 2013, pp. 2756-2759.

27. Vetter, Rio J., Justin C. Williams, Jamille F. Hetke, Elizabeth A. Nunamaker, and Daryl R. Kipke. "Chronic neural recording using silicon-substrate microelectrode arrays implanted in cerebral cortex." Biomedical Engineering, IEEE Transactions on 51, no. 6 (2004): 896-904.

28. Patterson, William R., Yoon-kyu Song, Christopher W. Bull, Farah L. Laiwalla, Arto Nurmikko, and John P. Donoghue. "CMOS ICs for Brain Implantable Neural Recording Microsystems." In CMOS Biotechnology, pp. 259-291. Springer US, 2007.

29. Patterson, William R., Yoon-Kyu Song, Christopher W. Bull, Ilker Ozden, Andrew P. Deangellis, Christopher Lay, J. Lucas McKay, Arto V. Nurmikko, John D. Donoghue, and Barry W. Connors. "A microelectrode/microelectronic hybrid device for brain implantable neuroprosthesis applications." Biomedical Engineering, IEEE Transactions on 51, no. 10 (2004): 1845-1853.

30. Song, Y-K., David A. Borton, Sunmee Park, William R. Patterson, Christopher W. Bull, Farah Laiwalla, John Mislow, John D. Simeral, John P. Donoghue, and Arto V. Nurmikko. "Active microelectronic neurosensor arrays for implantable brain communication interfaces." IEEE transactions on neural systems and rehabilitation engineering: a publication of the IEEE Engineering in Medicine and Biology Society 17, no. 4 (2009): 339.

31. Aceros, Juan, Ming Yin, David A. Borton, William R. Patterson, and Arto V. Nurmikko. "A 32-channel fully implantable wireless neurosensor for simultaneous

recording from two cortical regions." In Engineering in Medicine and Biology Society, EMBC, 2011 Annual International Conference of the IEEE, pp. 2300-2306. IEEE, 2011.

32. Yin, Ming, David A. Borton, Juan Aceros, William R. Patterson, and Arto V. Nurmikko. "A 100-channel hermetically sealed implantable device for wireless neurosensing applications." In Circuits and Systems (ISCAS), 2012 IEEE International Symposium on, pp. 2629-2632. IEEE, 2012.

33. Yin, Ming, Hao Li, Christopher Bull, David A. Borton, Juan Aceros, Lawrence Larson, and Arto V. Nurmikko. "An externally head-mounted wireless neural recording device for laboratory animal research and possible human clinical use." In 2013 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), pp. 3109-3114. IEEE, 2013.

34. Nurmikko, Arto V., Ming Yin, William R. Patterson, Juan Aceros, David A. Borton, and Farah Laiwalla. "Implantable wireless neural device." U.S. Patent Application 14/028,178, filed September 16, 2013.

Chapter 2. Custom Integrated Circuits for a Wireless Broad-band Neural Recording System

Extracellular neural signals, acquired either through penetrating microelectrodes or surface planar electrodes, are the most common source signals for Brain-Computer Interface applications due to their ability to provide the required spatiotemporal resolution for dynamic tasks. The magnitudes of these signals range from 10μV up to 1-2 mV [1, 2] and recording them with fidelity is a challenging task with unique constraints. This has led to the demand for custom neural signal acquisition amplifiers. Furthermore, broadband neural signal recordings generate data rates that are unprecedented in biomedical implantable devices, leading to the need for custom design for efficient data handling.

This chapter describes a full wireless broadband neural recording system, comprising 3 custom ICs. Design of the neural amplifier ASIC including full analog redesign for technology migration from 1.5 μm CMOS to 0.5 μm CMOS, scaling from 16 to 100 channel designs, simulation as well as benchtop performance and noise characterizations were completed as part of this work. Redesign of the data-handling digital controller chip involving changes to preexisting architecture to accommodate scaling from 16 to 100 channels as well as redesign of the RF clock

extraction comparator and design of a voltage regulator to support off-chip ADCs were also completed during this research. These design tasks are described in more detail in the next sections with the exception of the low-drop out voltage regulator design, which has been since been retired.

2.1 Neural Signal Acquisition

Signal-to-noise ratio (SNR) is a measure of the quality of a recorded signal, and is particularly important for robust decoding performance in neural sensing systems [3]. An SNR > 3 is the minimum performance specification for a recording system. Achieving this goal requires methodical optimization of system noise contributions, which are outlined below.

2.1.1 Noise in neural recording systems

There are 3 major contributions to system noise in a neural recording system:

i. *Thermal (Johnson-Nyquist) Noise:* This is the result of random movement of charge carriers in a conductor [4], and has a voltage spectral density given by 2.1:

$$v_{thermal}^2 = 4kTR \qquad \text{V}^2/\text{Hz} \tag{2.1}$$

where k is the Boltzmann constant, T is the absolute temperature, R is the equivalent resistance of the electrode and f is the frequency.

Both microelectrodes and transistors (channel conductors) experience thermal noise [5,6] , where current spectral density in the latter is given by 2.2.

$$i_{n-thermal}^2 = \frac{8}{3} kT g_m \qquad A^2/Hz \qquad \text{in strong inversion} \qquad (2.2)$$

where g_m is the transconductance, which in turn is dependent on size and gate over-voltage V_{GS}. When biased in weak inversion, however, the channel demonstrates shot noise instead (described below).

Nominal RMS thermal noise in a platinum microelectrode (with R = 100 kΩ and at a bandwidth of 10 kHz) is $\sim 4\mu V_{RMS}$. Since electrode thermal noise is a basic physical property that may not be mitigated, it is used as the upper bound specification for overall system noise.

ii. *Shot Noise:* The finite (quantized) nature of electric charge makes current flow across a semiconductor junction a Poisson process. The gives rise to white noise with a spectral density given by 2.3:

$$i_{shot}^2 = 2qI_D \qquad A^2/Hz \qquad (2.3)$$

This may generally be ignored in strong-inversion but becomes an important source of noise in sub-threshold MOSFET operation.

iii. *Flicker Noise:* This is generally thought to be related to trapped charge carriers in the transistor gate oxide, and is inversely proportional to both transistor area and frequency (the latter leading to it being referred to as *1/f* noise). The voltage spectral density of flicker noise is given by 2.4; this is a critical noise source for neural amplifiers, and drives the sizing of the input transistors.

$$v_{n-1/f}^2 = \frac{K_F}{C_{ox} W L f^{\alpha}} \qquad V^2/Hz \qquad (2.4)$$

PMOS transistors in p+ bulk silicon reportedly have lower flicker noise due to a wider separation between gate oxide interface and the deeper p+ channel. P-channel input-transistors are thus favorable for amplifier noise optimization.

2.1.2 Design of a multichannel Neural Signal Amplification ASIC

The neural signal amplifier described in this section is designed for broadband signal acquisition. As such, it has a bandwidth from 1 mHz to 7.8 kHz (spanning both Local-Field Potential (LFP) and Single-Unit Activity (SUA) domains). Signal amplitudes are in ~20 μV to 2mV range, and this sets the amplifier's maximal noise constraints.

The overall ASIC architecture for a 100-channel system is shown in Figure 2.1. Each channel has a dedicated low-noise amplifier, whose output is multiplexed into one of two unity-gain output buffers, each in turn driving a separate ADC. This architecture also allows for a single ASIC to interface with up to two microelectrode arrays providing for greater flexibility.

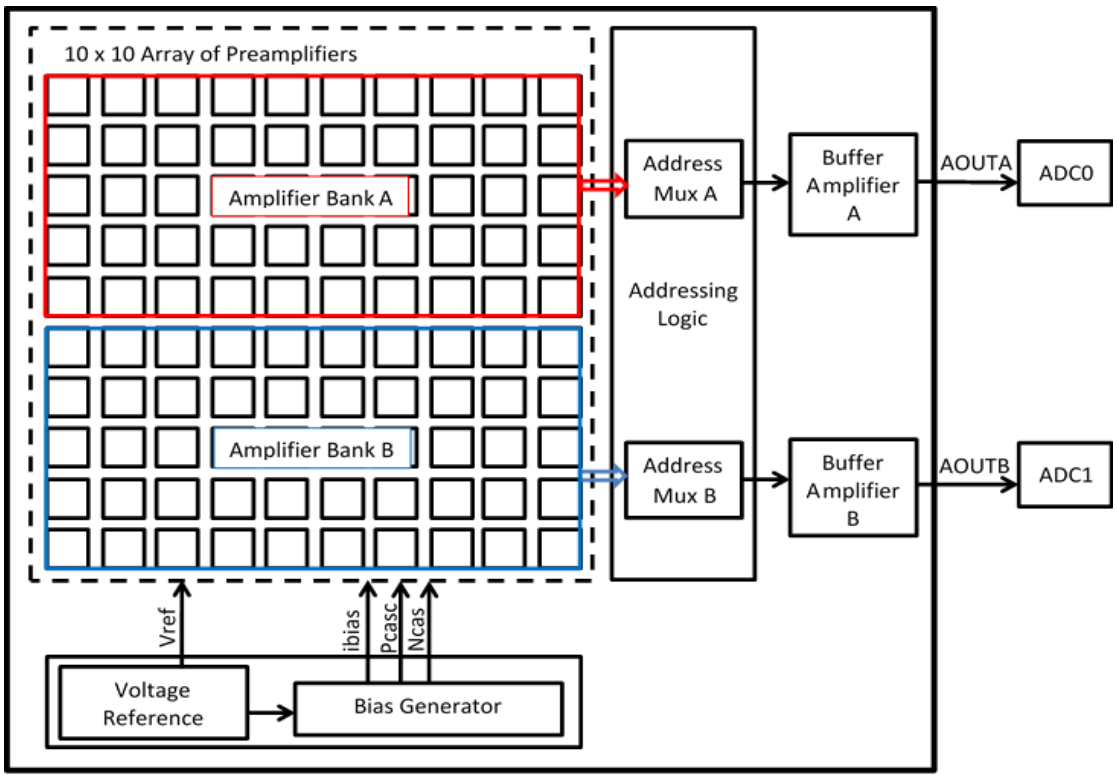


Figure 2.1: Overview Diagram of Amplifier ASIC

The low-noise, high-bandwidth neural signal amplifier is implemented using a folded-cascode operational transconductance amplifier (OTA) topology. This approach was first described by Harrison et al in [7] and its use is widely reported in neuroengineering literature [8]. Figure 2.2 shows the overview schematic of the preamplifier, which comprises the OTA, active feedback circuitry and a single-stage source follower output buffer.

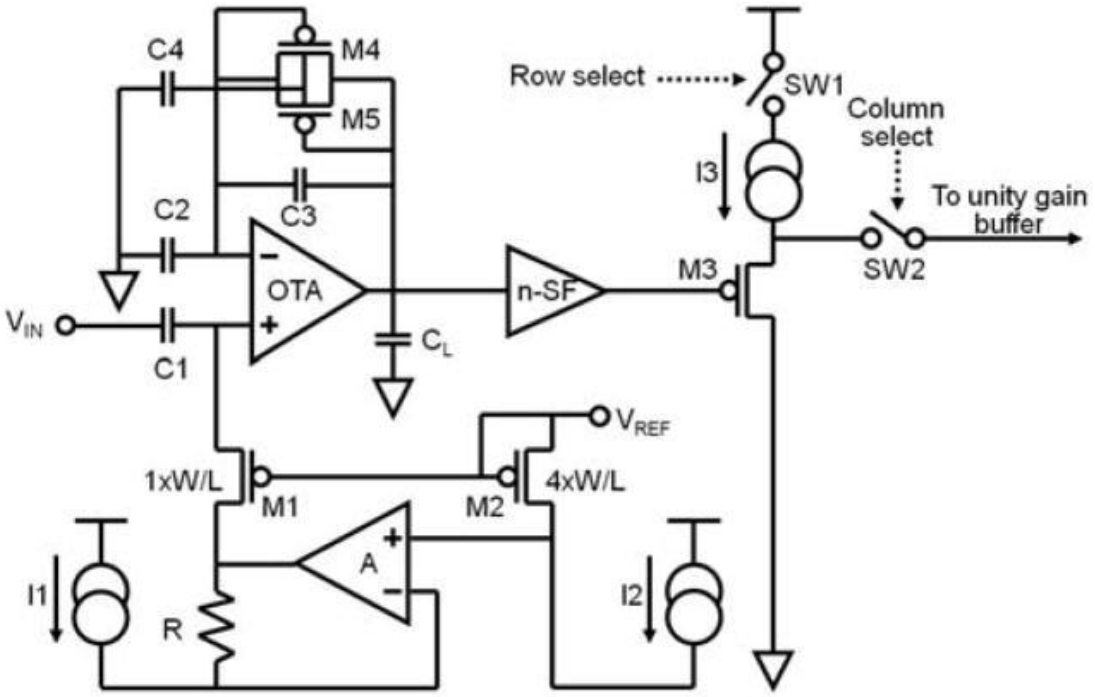


Figure 2.2: Neural Signal Amplifier. Implemented as an OTA with active Feedback.

Figure 2.3 demonstrates the transistor level details of the folded cascode OTA. Robust rejection of the electrode-tissue interface DC potential is a critical aspect of amplifier design, and is accomplished through an on-chip High-pass filter comprising the input capacitor and a tunable MOS "pseudoresistor" element for a very low cutoff- frequency in the mHz- Hz range. Amplifier gain is set by the ratio of feedback capacitor C3 and the input capacitor C1, which are sized to provide a mid-band gain A_M of 46 dB as shown by the open-loop AC analysis results in Figure 2.4. Load capacitance C_L sets the high-frequency cutoff and is selected to provide a high-frequency pole at 7.8 kHz in this design.

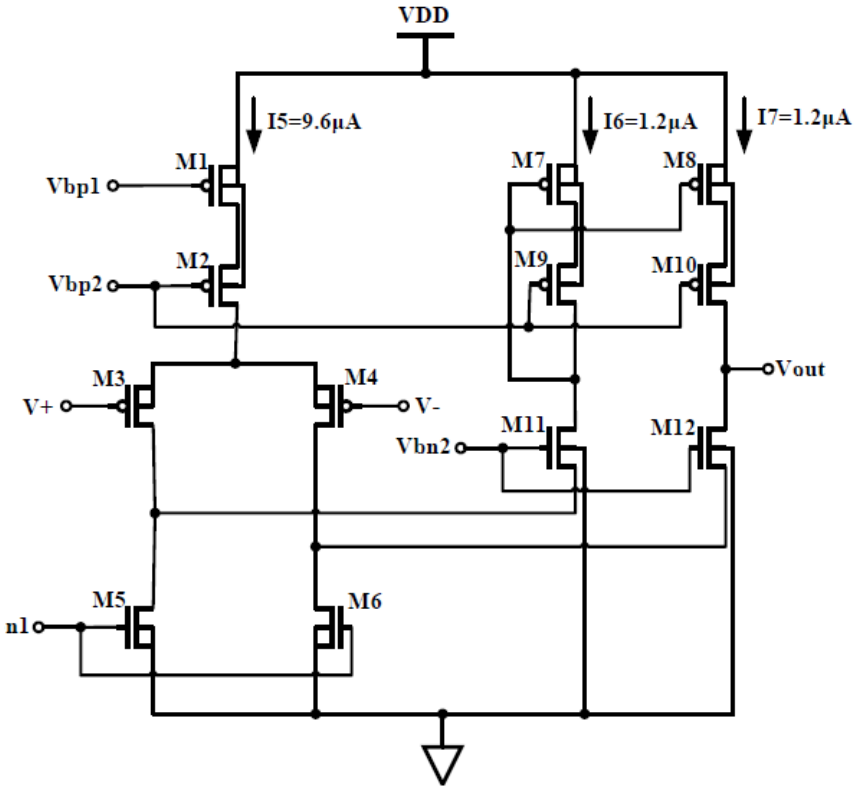


Figure 2.3: Folded Cascode CMOS Operational Transconductance Amplifier. From [10].

The amplifier is designed to work off a single-ended power supply (a 3.7 V battery in this case). A pair of diode-connected PMOS (M4 and M5 in Figure 2.2) are used to set the DC bias point of the amplifier to ½ the power supply enabling bidirectional output swing. A large capacitor C4 is added in parallel to the source-bulk terminals of these PMOS to mitigate the impact of their parasitic capacitances on feedback capacitance and amplifier gain.

Amplifier noise is optimized by using large (960 µm/1.5 µm) PMOS devices biased in weak-inversion. Total voltage noise spectral density for the amplifier in subthreshold operation is given 2.5:

$$v_n^2 = \frac{4k_BT}{\kappa g_{m3}}\left(1 + \frac{g_{m5}}{g_{m3}} + \frac{g_{m7}}{g_{m3}}\right) \qquad \text{V}^2/\text{Hz} \qquad (2.5)$$

where k_B is the Boltzmann constant, T is absolute temperature and κ is a process-dependent subthreshold parameter, empirically determined to be ~0.7 in our process. g_{m3} is the transconductance of the input transistor, g_{m5} is the transconductance of the NMOS source and g_{m7} is the transconductance of the PMOS in the second stage cascode.

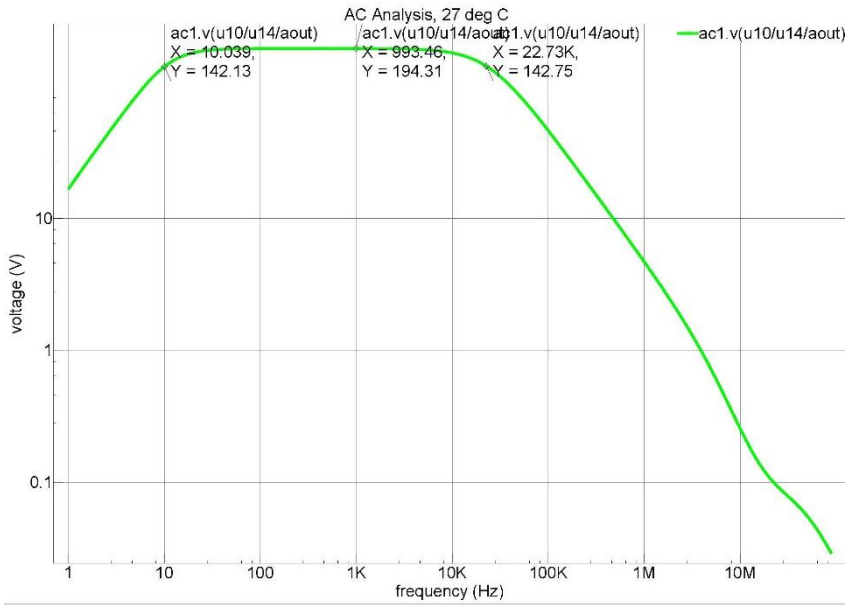


Figure 2.4: Open-loop Gain response of Neural Signal Amplifier OTA.

Design of a well-controlled tunable pseudoresistor is another crucial design component. This is a nominally off MOSFET, and several designs are reported in literature [7, 8, 11]. Non-linearities in pseudoresistor performance produce output distortion which is undesirable. Process-dependent variation in threshold voltage V_{TH} is a one significant cause for non-linearity, since the current-voltage relationship of a MOSFET in subthreshold regime is exponential, as shown in (2.6) [12]:

$$I_D = I_o e^{\frac{V_{GS}-V_{TH}}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \tag{2.6}$$

where I_o is the subthreshold current constant, n is the subthreshold slope factor and V_T is the thermal voltage.

The effective resistance of a sub-threshold MOS is then given by (2.7), and depends on device V_{GS}. If this V_{GS} is set reliably (through use of active feedback in this case), it produces a well-controlled R_M.

$$R_M = \frac{V_T}{I_o e^{\frac{V_{GS}-V_{TH}}{nV_T}}} \tag{2.7}$$

The pseudoresistor implementation is shown in Figure 2.2. M1 and M2 are PMOS devices (with a size ratio of 1:4) driven by scaled copies of the same current source. Mp2 is diode-connected, and the gates of both devices are biased at a known sub-threshold voltage V_{ref}. The feedback amplifier then sets the source voltage of Mp1 to satisfy 2.8 below:

$$V_{GS1} + I_1 R = V_{GS2} \tag{2.8}$$

The effective resistance of R_{M1} is then driven by the ratio of the sizes of M1:M2 and is independent of threshold voltage, as given by 2.9:

$$R_{M1} = \frac{4V_T e^{\frac{I_1 R}{V_T}}}{I_1} \tag{2.9}$$

Implementing R on-chip makes it susceptible to process variations. It is thus implemented off-chip, which also allows it to be used to tune R_{M1} according to the desired high-pass frequency cut-off. The OTA output is fed into a source follower buffer stage, followed by a class AB unity gain buffer stage, which are described is detail in [10].

The Amplifier ASIC is implemented in ON-Semi 0.5 μm CMOS process. Tanner Design Suite is used for layout and SmartSpice™ is used for simulations. A single amplifier channel consumes 54 μW of power from a 3.3 V supply. It has a simulated common-mode rejection ratio (CMRR)> 60 dB and a power supply rejection ratio (PSRR) > 50 dB.

Figure 2.5 shows a photomicrograph of the ASIC, which is implemented as a 10x10 grid of preamplifiers with a 400 μm pitch to enable direct integration onto a substrate via flip chip or ball-grid array bonding.

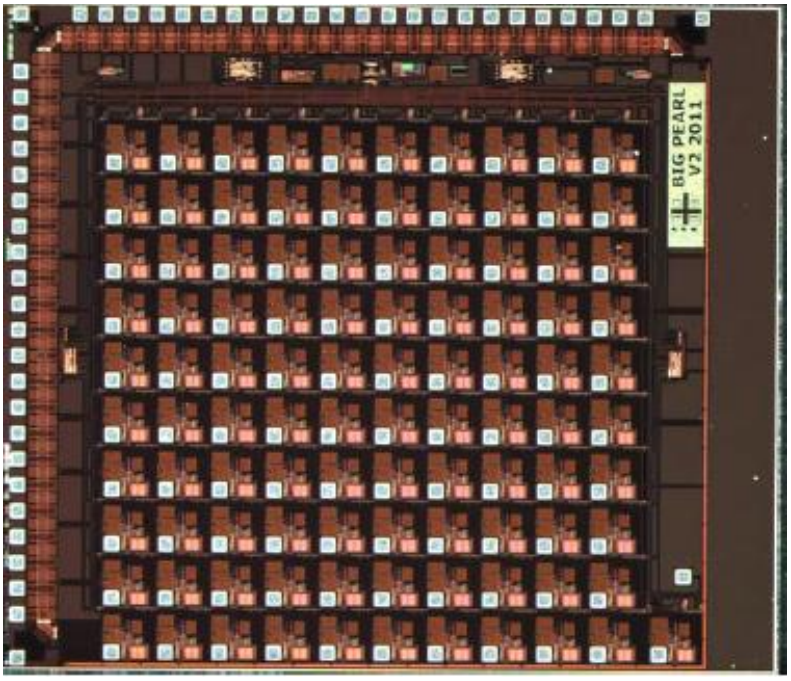


Figure 2.5: Photomicrograph of 100-channel Chip.

2.1.3 Bench-top Performance Testing and Noise Analysis

A packaged amplifier ASIC was used for benchtop characterizations of performance. Amplifier gain was characterized at different high-pass cutoff frequencies by sourcing a 1kHz sinusoidal waveform from a bench top function

generator (though a signal attenuator). Amplifier output was measured using a Tektronix oscilloscope. This is shown in Figure 2.6.

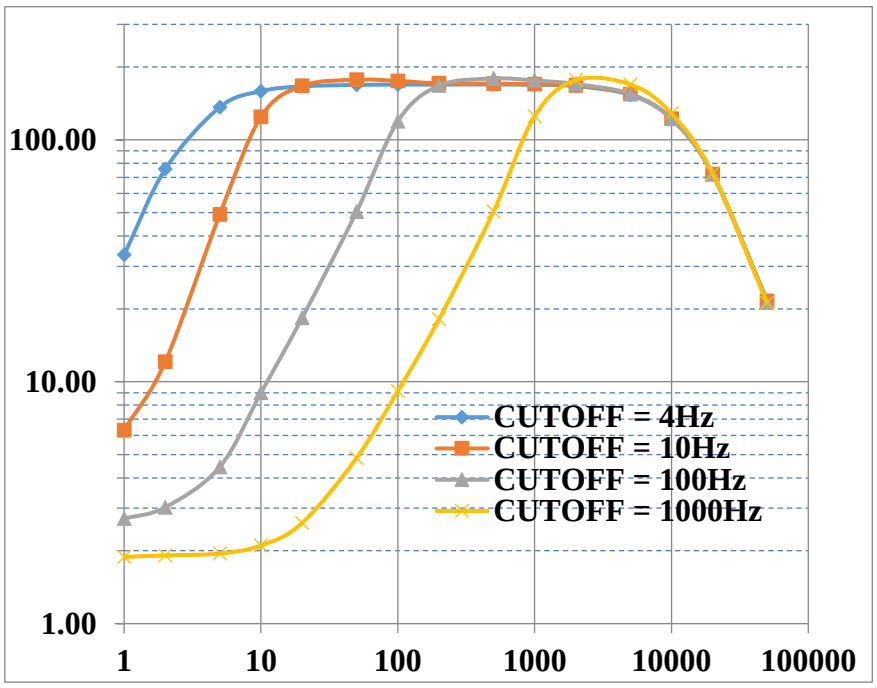


Figure 2.6: Bench top gain characterization of Neural Signal Amplifier

Input-referred amplifier noise was measured by grounding the amplifier input and measuring the amplifier output using a National Instruments DAQ. The chip was powered with a battery to minimize 60 Hz noise coupling. This setup and measurement are shown in Figure 2.7.

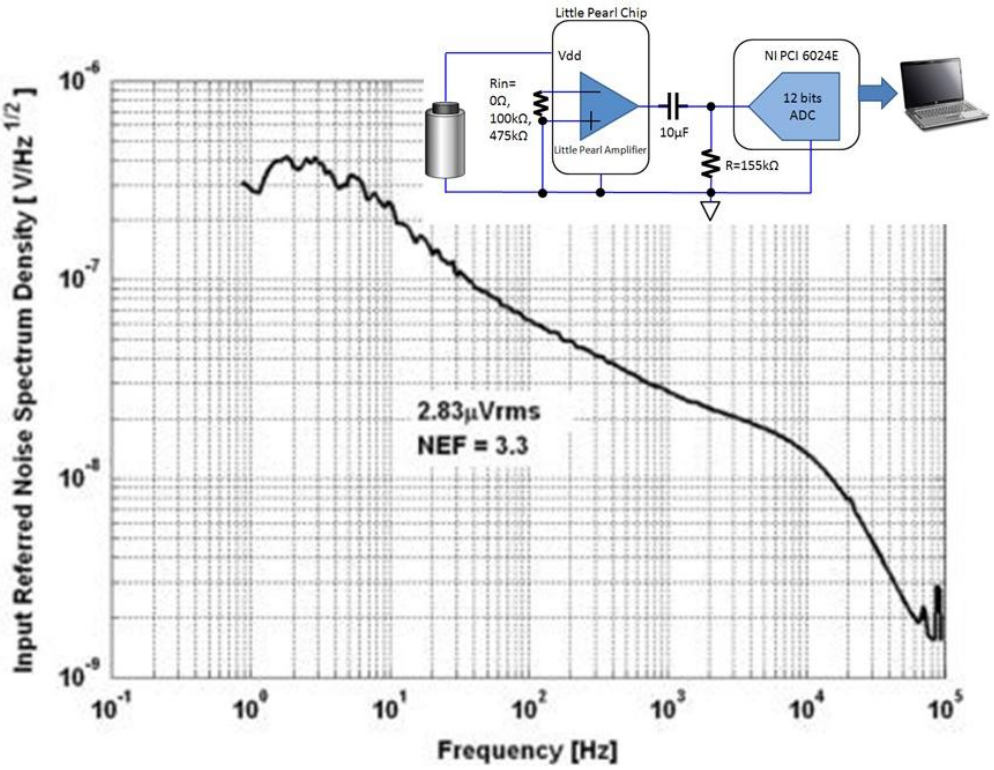


Figure 2.7: Input-referred Amplifier Noise. Inset shows measurement setup.

2.2.3 CMOS Technology Migration: A Perspective

The amplifier chip described above has undergone extensive evolution over a 10 year span. The first design was implemented as a 16 channel system with a single ADC interface using the AMI 1.5 μm CMOS process [10]. Retirement of this fabrication process and the anticipated need for eventual upscaling to 100 channels were the primary driving factors leading to redesign of the amplifier in the 0.5 μm CMOS process (which is described above). While digital circuitry was easily scaled using synthesis tools with the new technology's standard cell library, analog redesign required an in-depth analysis of transistor sizes, transconductances and drain currents. Analog scaling approaches have received some attention in literature [13-15], but are largely selected according to the application. Given the focus on low-power and low-noise in our application, this redesign effort focused on maintaining V_{GS} and I_D for

each transistor. These were first determined through DC operating-point simulations, and redesigned with the assistance of foundry-furnished process parameter listings (such as oxide capacitance C_{ox}, Threshold voltage V_{TH} and device conductance β, sheet capacitance and resistivities). The full spreadsheet of this analysis is included as Appendix II. Devices were sized according to this analysis, and validated using simulation at the schematic level. Layout was manually updated, and verified using the Layout versus Schematic tool.

In the 1.5 μm process, silicon real-estate was the limiting factor for amplifier gain and noise performance (due to area constraints on the input transistor and capacitor, given a 400 μm x 400 μm footprint). Area savings from scaling (approximately 50%) were used to optimize these parameters. Amplifier gain was in increased from 42 dB to 46 dB while input referred RMS voltage noise was reduced from 9 μV-rms to 4.5 μV-rms.

2.2 Data Management and Digitization

Data from the 100-channel amplifier ASIC is digitized using two off-the-shelf 12-bit ADCs from Linear Technology. Digitized data is interleaved and Manchester-coded prior to transmission. This data management is performed by the Digital Controller ASIC, which manages both Amplifier ASIC sampling and ADC timing. An overview of the Controller ASIC is shown in Figure 2.8, and its various functions are described in more details below:

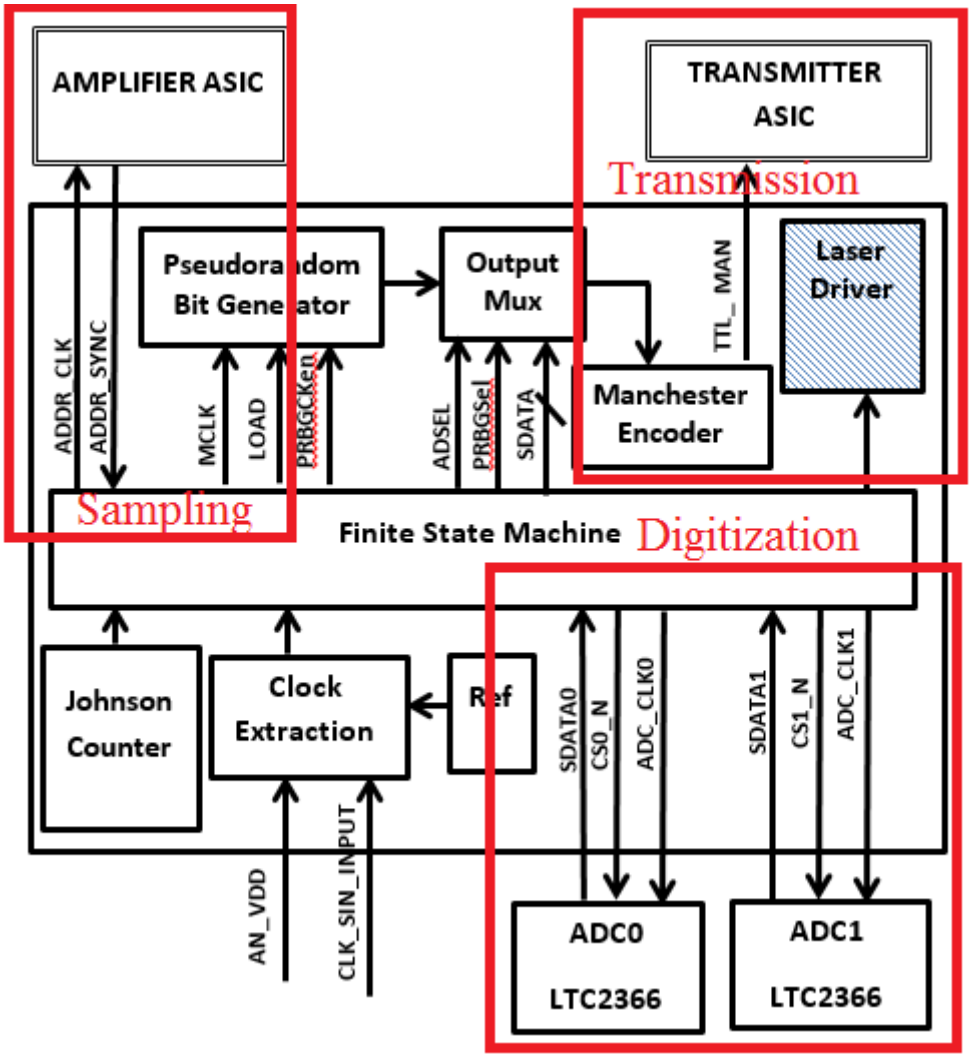


Figure 2.8: Block Diagram of the Digital Controller ASIC

: System clock may either be provided through an off-chip 48 MHz crystal oscillator or extracted from RF-coupled power. With the exception of the Manchester encoder, all other subsystems use ½ the oscillator frequency (24 MHz); this is generated using an on-chip clock division circuit. In the RF-powered scenario, system clock is extracted from a 200 mV sinusoidal (at the RF-carrier frequency) using an on-chip clock extraction comparator. The schematic of this Clock-extraction Comparator is shown in Figure 2.9.

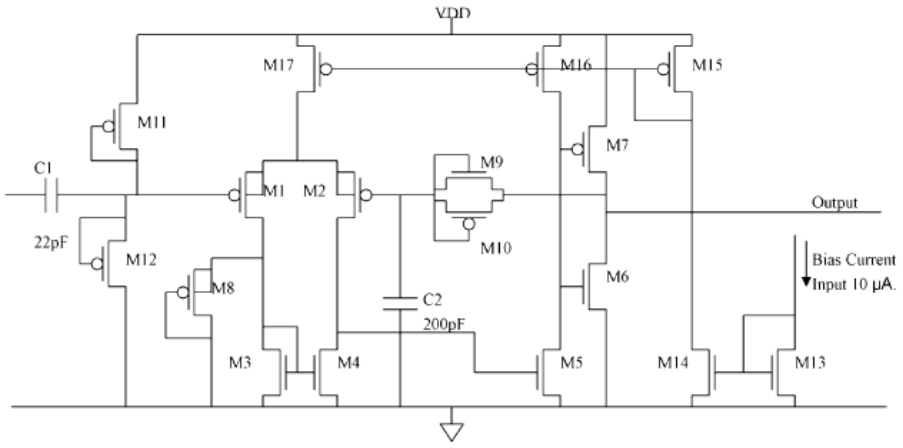


Figure 2.9: Clock Extraction Comparator. From [10].

The clock comparator is a 2-stage differential amplifier followed by a conventional inverter. The input is capacitively coupled, and DC bias level is set at 40-60% of power supply though the DC filtering network comprising M9, M10 and C2. These FETs source or sink current from the capacitor depending on output voltage, and their sizes may be chosen to design for a 50% duty cycle. The comparator's frequency response sets the limiting clock rate to 30MHz; it is thus not usable with a Manchester Encoded data stream due to bandwidth limitation, but is used in both non-encoded and optical output systems.

i. *ADC Control:* The 12-bit ADCs from Linear Technologies operate at 1.5 Mbps and have a 2-clock-cycle lead time per conversion cycle (14 clock cycles per each 12-bit sample). The Controller ASIC manages the timing of channel multiplexing so as to eliminate this 2-cycle lag from ADC overhead by overlapping the ADC activation intervals.

ii. *Front-end-multiplexing:* Amplifier channels are multiplexed through 2 output buffer amplifiers. The Controller ASIC drives the amplifier multiplexor

switching to account for both amplifier follower stage settling times as well as ADC sample time. The frequency of this multiplexing clock is set at 1/24 of the ADC clock (set by the system specifications of 20ksamples/second/channel x 50 channels/multiplexor).

iii. *Data-packet construction*: A full data frame from the recording system comprises a single sample from each of the 100 amplifiers. A 24-bit identifier synch sequence is inserted into the data stream after transmission of each frame to enable alignment at the receiver. Synch is inserted in response to a signal from the amplifier chip which keeps track of when the last channel is sampled. Channel multiplexor clock is suspended for 24 clock-cycles while synch is being transmitted yielding an effective sampling rate of 19.6 kHz/channel.

iv. *Telemetry:* The datastream may either be transmitted optically using a fast (> 1 Gbps) Vertical Cavity Laser (VCSEL) operating at 800 nm or through 3-5 GHz modulated RF. Optical transmission of TTL data is facilitated by a laser-driver providing up to 3mA of current while an IEEE 802.3 Manchester encoder prepares the datastream for high-integrity RF transmission.

The Digital Controller ASIC is designed in ON-SEMI- 0.5 μm CMOS. Figure 2.10 Shows the top-level layout for the chip, which occupies 2 mm x 2 mm and consumes 1mW from a 3V supply. ADC, amplifier channel multiplexing and Manchester encoder function is verified with bench-top testing on a packaged device.

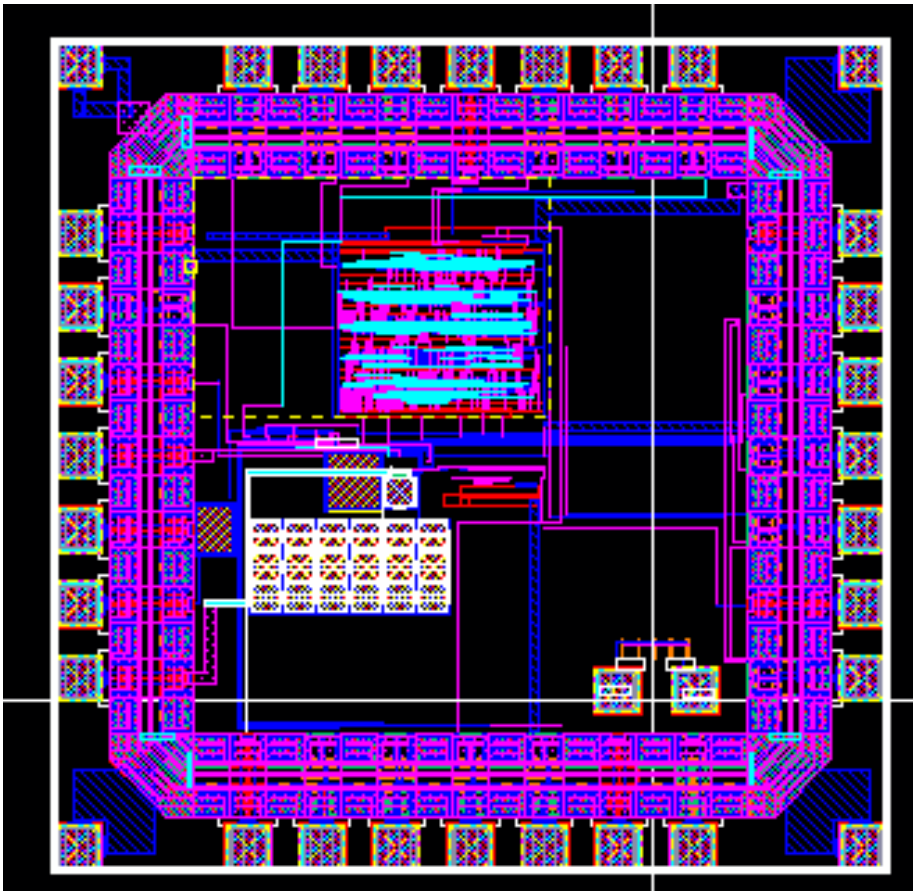


Figure 2.10: Top level layout of the Digital Controller Chip

2.3 Data Transmission

The 48 Mbps Manchester encoded datastream is wirelessly transmitted using a custom RF ASIC which operates at a nominal frequency of 3.5 GHz. It is capable of using either On-Off Keying (OOK) or Binary-Phase-Shift-Keying (BPSK) for minimization of transmission bit-error rates (BER). Data rates up to 100 Mbps are supported with a nominal 35% efficiency. Output power is user-tunable from 4-16 mW depending on desired transmission distance. Details of this ASIC are described in [21].

These three ASICs, along with the COTS ADCs, Crystal Oscillator and discrete passive components comprise fully wireless neural recording systems which

have been extensively tested in in-vivo work described in [20] and [21]. These are however “reporter” devices with neither the ability to interrogate the implant nor the capability to communicate information back to the system. Addition of such features is very desirable for the next-generation neuroprosthetic device. The next 3 chapters describes advances made in these arenas by research conducted for this thesis.

2.4 References

1. Buzsáki, György, Costas A. Anastassiou, and Christof Koch. "The origin of extracellular fields and currents—EEG, ECoG, LFP and spikes." Nature reviews neuroscience 13, no. 6 (2012): 407-420.

2. Gold, Carl, Darrell A. Henze, Christof Koch, and György Buzsáki. "On the origin of the extracellular action potential waveform: a modeling study." Journal of neurophysiology 95, no. 5 (2006): 3113-3128.

3. Suner, Selim, Matthew R. Fellows, Carlos Vargas-Irwin, Gordon Kenji Nakata, and John P. Donoghue. "Reliability of signals from a chronically implanted, silicon-based electrode array in non-human primate primary motor cortex." Neural Systems and Rehabilitation Engineering, IEEE Transactions on 13, no. 4 (2005): 524-541.

4. Huigen, E., A. Peper, and C. A. Grimbergen. "Investigation into the origin of the noise of surface electrodes." Medical and biological engineering and computing 40, no. 3 (2002): 332-338.

5. Tsividis, Yannis. "Operation and Modeling of the MOS Transistor." (2003).

6. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, New York, NY, 2001

7. Harrison, Reid R., and Cameron Charles. "A low-power low-noise CMOS amplifier for neural recording applications." Solid-State Circuits, IEEE Journal of 38, no. 6 (2003): 958-965.

8. Jochum, T., Denison, T. and Wolf, P., 2009. Integrated circuit amplifiers for multi-electrode intracortical recording. Journal of neural engineering, 6(1), p.012001.

9. Gosselin, Benoit. "Recent advances in neural recording microsystems." Sensors 11, no. 5 (2011): 4572-4597.

10. Patterson, William R., Yoon-kyu Song, Christopher W. Bull, Farah L. Laiwalla, Arto Nurmikko, and John P. Donoghue. "CMOS ICs for Brain Implantable Neural Recording Microsystems." In CMOS Biotechnology, pp. 259-291. Springer US, 2007.

11. Yin, Ming, and Maysam Ghovanloo. "A low-noise preamplifier with adjustable gain and bandwidth for biopotential recording applications." In Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on, pp. 321-324. IEEE, 2007.

12. Aceros, Juan, Ming Yin, David A. Borton, William R. Patterson, and Arto V. Nurmikko. "A 32-channel fully implantable wireless neurosensor for simultaneous recording from two cortical regions." In Engineering in Medicine and Biology Society, EMBC, 2011 Annual International Conference of the IEEE, pp. 2300-2306. IEEE, 2011.

13. C. Galup-Montoro, M.C. Schneider, and R. Coitinho, "Resizing Rules for MOS Analog-Design Reuse," IEEE Design &Test, *vol*. 19, no. 2, Mar./Apr. 2002, pp. 50-58.

14. *R. Castro-Lopez et al.,* Reuse-Based Methodologies and Tools in the Design of Analog and Mixed-Signal Integrated Circuits, Springer, 2006.

15. T. Levi et al., "Scaling Rules for MOS Analog Design Reuse," Proc. Int'l Conf. Mixed Design of Integrated Circuits and Syste*m* (MIXDES 06), IEEE Press, 2006, pp. 378-382.

16. T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 2nd ed., Cambridge University Press, 2003.

17. M. Pelgrom and M. Vertregt, CMOS technology for mixed signal ICs," Solid-State Electronics, vol. 41, pp. 967{974, 1997.

18. T. DeMassa and Z. Ciccone, Digital Integrated Circuits, John Wiley and Sons, 1996.

19. R.J. Baker, H.W. Li, and D.E. Boyce. CMOS Circuit Design, Layout, and Simulation, Series on Microelectronic Systems, IEEE Press, 1998.

20. Yin, Ming, David A. Borton, Juan Aceros, William R. Patterson, and Arto V. Nurmikko. "A 100-channel hermetically sealed implantable device for chronic wireless neurosensing applications." Biomedical Circuits and Systems, IEEE Transactions on 7, no. 2 (2013): 115-128.

21. Yin, Ming, Hao Li, Christopher Bull, David A. Borton, Juan Aceros, Lawrence Larson, and Arto V. Nurmikko. "An externally head-mounted wireless neural recording device for laboratory animal research and possible human clinical use." In Engineering in Medicine and Biology Society (EMBC), 2013 35th Annual International Conference of the IEEE, pp. 3109-3114. IEEE, 2013.

Chapter 3. Long-term Monitoring of Chronic Implants

Chapter 2 described ASICS for active implantable sensors thatare part of Neural recording systems. Microelectrode array and microwire based platforms focusing on neural ensemble recordings have been validated in various animal models over the last two decades [1-7]. The long-term implantable BCIs reported in literature have been exclusively based on passive sensors with percutaneous connections to external electronics. Though infection risk through the skin opening remains the leading cause of complication in these devices, tethering-associated inflammation has also been implicated in long-term recording quality and reliability.

One of the problems consistently reported by research groups using passive penetrating electrodes is the variability and degradation of signal quality over time. Suner et al have quantified this variation on the basis of channel SNR, and found that channel SNR can vary up to 30% from day to day, and is often associated with changes in electrode impedance [3]. This channel variability adds to the burden on decoder training in clinical BCIs [8].

Continual degradation of recording performance has also been reported by several studies [4,5]. The mechanism of these phenomena are not well-understood, but have been attributed to a mix of electrode-surface electrochemical and physiological factors [9-12]. This is of interest to both neuroimmunologists and

material science researchers. Studies of tissue-electrode interface impedance changes in the post-implant period have offered some interesting insight [11, 12], suggesting that brain micromotion against a tethered rigid electrode may be responsible for some of the observed changes, and that complex impedance spectroscopy may be a useful technique to characterize this response.

Implanted Non-human and human primates are the best models for studying chronic post-implant processes. There is however currently a dearth of appropriate tools to interrogate these implants, with the exception of 1 kHz impedance measurements and postmortem histopathology. The possibility to continually interrogate the likely dynamic tissue-electrode interface thus offers an exciting opportunity. The characterization of the dielectric properties of biological systems via impedance spectroscopy has historic precedent in neuroscience [23-29], and particularly in in BCI research where it has yielded informative results.

3.1 Electrode-Tissue Interface (ETI)

The electrode-tissue interface is a dynamic entity which has contributions from metallic, ionic and cellular components. Figure 3.1 shows a proposed electrical model of the interface [30], and demonstrates that the electrode and the cellular compartments are each modeled has having both resistive and capacitive features.

At the metal-electrode-electrolyte interface, capacitive contributions come from the “double layer capacitance”, which is a consequence of charge carriers lining up at the phase boundary [31-33] as demonstrated in Figure 3.2. Resistive

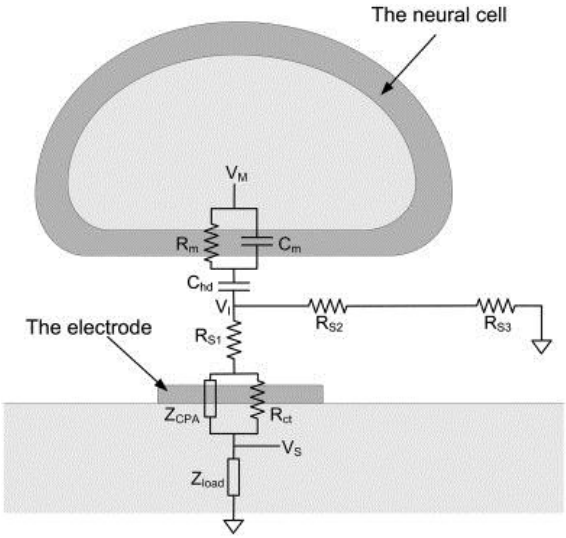


Figure 3.1: Electrical model of the Tissue Electrode Interface

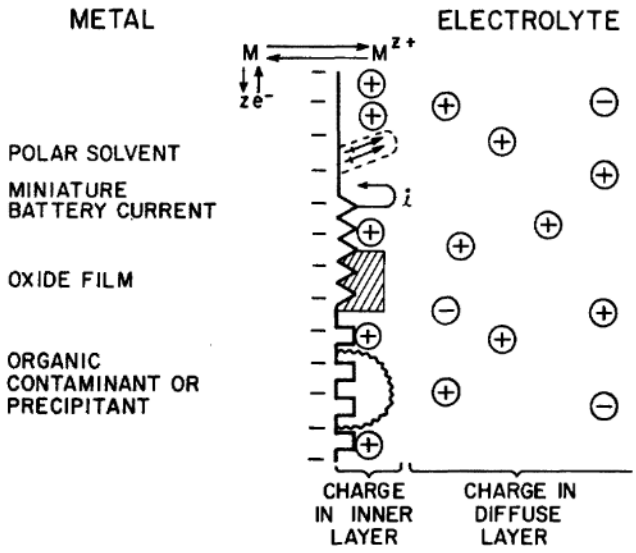


Figure 3.2: Cross Section view of a metal electrode-electrolyte interface. From [32]

contributions come from Charge-transfer resistance R_{CT} and Warburg impedance element, there the is a (associated with ion absorption into the interface) and is considered of particular important in frequencies of interest in biology. This gives rise to an overall electrode-electrolyte impedance given by 3.1:

$$Z = \frac{R_{CT}}{1+j\omega^{\beta}K/R_{CT}} \tag{3.1}$$

where K and β are measures of electrode surface smoothness.

Cellular components make contributions to Impedance through their volume conductor "resistive" properties. The cell membrane demonstrates capacitive features due to its hydrophobic core while ion channels contribute "leakage currents".

Cellular components also make significant dynamic contributions to the interface impedance through inflammatory responses as part of the Foreign Body Reaction to implanted materials. Astrocytes and microglia, two types of neuro-immune cells (shown in Figure 3.3) are implicated in this process [28, 34, 35]. These are thought to render the blood-brain barrier "leaky" as part of the chronic inflammation cascade[36].

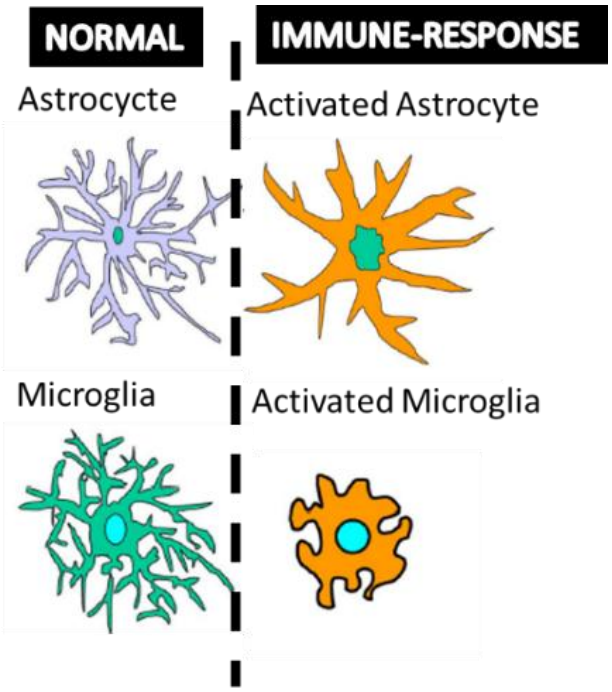


Figure 3.3: Glial cells in the brain at rest (Left) and after being activated in response to injury (Right)

Physiologic immune response has a well-characterized temporal course, leading to thick scar formation in ~ 3 weeks [34]. Significant changes in impedance are observed during this period, and the use of this technique has yielded prolific insight about tissue reaction. Its non-invasive nature makes it a good technique to use in a chronic implant. Furthermore, its standard use in a variety of disciplines means that there is already a large body of data that analysis of neural data may be able draw from. Recent studies are even beginning to unravel specific impedances signatures for parts of the foreign body reaction in the brain [38,39]. The next section describes the technique as well as our implementation of the technique.

3.2 Impedance Spectroscopy: Theory and Application

Electrochemical Impedance Spectroscopy (EIS) is a technique that was originally developed characterization of material dielectric properties by chemists but has found widespread utility in biological applications [23-25,41] including neuroscience [26,27]. The technique is based on using a small-signal measurement of the linear electrical response of a material of interest (including electrode effects) and the subsequent analysis of the response to yield useful information about the physicochemical properties of the system [40].

The analysis of biological systems with this technique has shown that there are distinct identifiable signatures associated with various parts of the interface. Figure 3.4 shows a plot of the implicated processes as a function of frequency. In the context of neural signal acquisition, this suggests that impedance spectra of the interface may

be able attribute the changing impedance to specific components. The consequences of this, though, exceed the mere diagnostic value. The possible benefits of using impedance spectroscopy in the neural recording systems are outlined below:

i. In the acute surgical setting, impedance spectral features may help characterize the success (and anatomical placing of the electrode array) by distinguishing between the predominantly resistive CSF from the more capacitive cortex.

ii. It may provide a comprehensive picture of the interface, allowing for possible use in selection of signals for decoder implementations

iii. By elucidating the cellular mechanisms at the interface, it may guide the development of electrode surface modification approaches as well provide insight into possible immunomodulatory solutions.

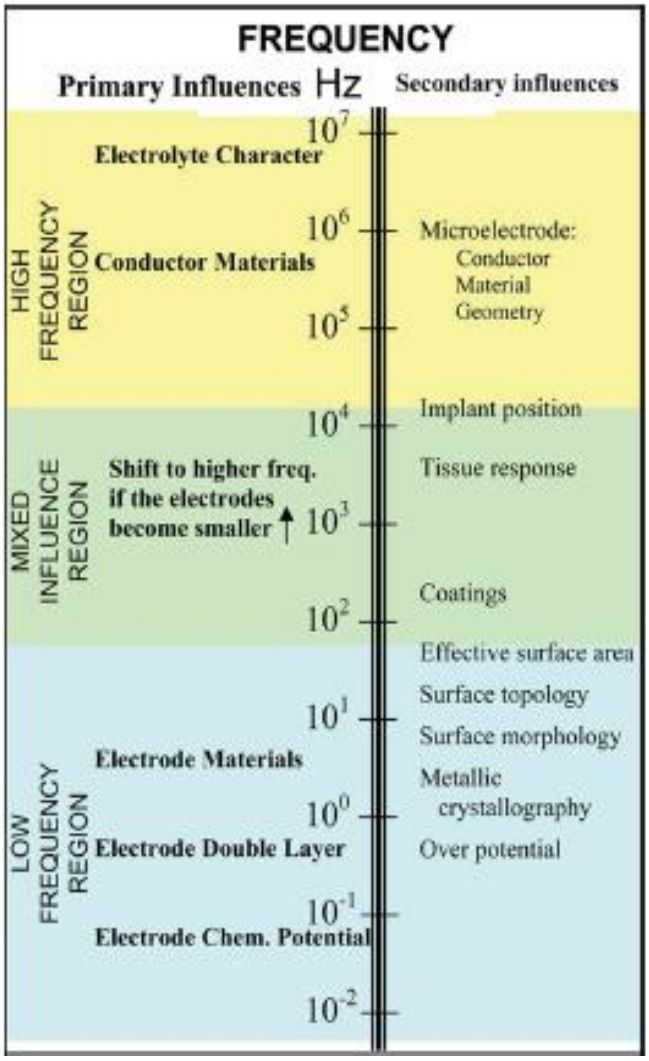


Figure 3.4: Electrochemical processes detected by impedance spectroscopy

3.2.1 Impedance Spectroscopy: Circuit Implementations

Impedance is defined as the opposition to current flow under the influence of a changing electric field. Quantifying electrode impedances thus relies on the availability of a robust AC signal source of predetermined amplitude and frequency. This has been implemented in a finite way in current neurotechnology: commercial neural recording systems such as Blackrock Cerebus™ and Plexon NanoZ™ Data acquisition systems obtain impedance data at 1 kHz from their neural probes respectively. The accomplish this by applying a sinusoidal voltage of known

magnitude across the tissue interface through the reference electrode and measuring the frequency response of the unknown impedance Z(jω) at the recording amplifier input nodes. Figure 3.5 demonstrates the circuit configuration for making this measurement.

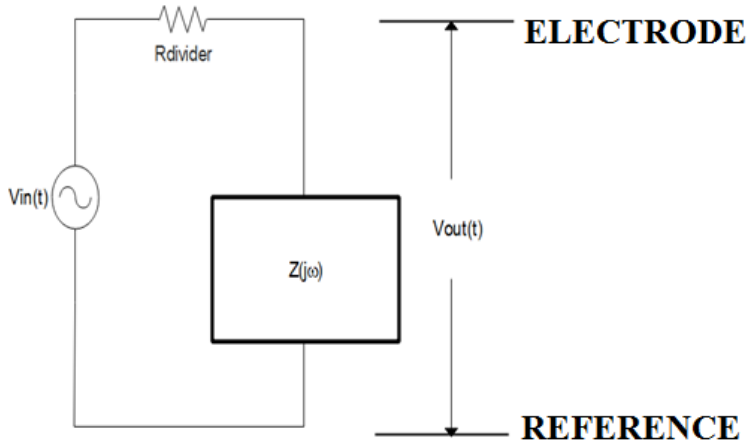


Figure 3.5: Circuit diagram for impedance measurement

where $V_{in}(t)$ is the AC source of a predetermined voltage and frequency. $R_{divider}$ is a known calibration resistance and Z(jω) is the unknown impedance, which in this case is the electrode-tissue-interface. The transfer function of the circuit in Figure 3.9 is given by 3.4:

$$V_{out}(t) = \frac{Z(j\omega)}{R_{divider}+Z(j\omega)} V_{in}(t) \qquad (3.2)$$

The calibration resistance $R_{divider}$ forms a simple resistive divider with the unknown impedance Z(jω) , and the measured attenuation of the source voltage $V_{in}(t)$ can be used to calculate Z(jω). Impedance is a complex quantity but it is typically the absolute magnitude |Z(jω)| which is computed in commercial systems (although the NanoZ does provide phase information). Capturing phase is important because data suggests that dynamic changes at the interface may be coded by the phase of the

impedance response. The resolution of capacitive vs resistive contributions may be an important tool even at single frequencies, aiding in attributing signal changes to cellular vs electrode-related processes.

Incorporating multi-frequency impedance measurements on an ASIC offer promising prospects for data to understand interfacial changes. The implementation would rely an on-chip tunable voltage source to generate voltage stimuli with well-characterized frequency content. This may be distributed to individual electrodes through a multiplexing system, allowing for focal characterization if needed. Furthermore, it would be integrated on to the neural recording amplifier ASIC platform minimizing the overheads of the design. This is the approach we have chosen, and it is described in further details in the sections below.

The design of sub-megahertz sinusoidal voltage sources or "oscillator circuits" is well-described in literature. We have implemented an integrated Wien bridge oscillator to serve as the sinusoidal voltage source. The rest of the ASIC design is based on some systems level considerations, which are described below.

3.3 Design considerations in developing an integrated impedance-spectrometry ASIC

Implantable biomedical ASIC design tends to be a conservative endeavor. When any expansions are made to the capabilities of a system, special consideration must be given to the possible impact it may have on the existing system, and the design needs to carefully mitigate these interactions. The best approach to added

functionality is to design each function as an independent module, which may be turned off to essentially become invisible to the rest of the system. The major characteristics of this type of modular design are outlined in the following section

3.3.1 Modular approach to ASIC design:

The basic design principle for modularity is independent control of the module without any impact on the main purpose of the chip. In our case, this translates into the ability to continue recording neural data seamlessly in the event of a malfunction in the impedance spectroscopy module. Our design has ensured this as follows:

i. *Independent power supply*: The impedance measurement module (IMM) receives power through a separate dedicated power line, which may be turned off to revert the ASIC to recording mode. This shut-off mechanism also allows for power-savings when the IMM functionality is not being used.

ii. *Emergency shut-off via Reset switch*: The Impedance measurement module has a dedicated reset-line which can override any internal delays and allows for fast shutoff in case of malfunction.

iii. The design should allow for probing intermediate signals, and have the capability to bypass sub-circuits if a partial dysfunction occurs in one of the sub-circuits. This is implemented through routing these signals to chip pads where they are connected via jumpers (or alternatively routed to external signal sources).

3.4 Sine-wave based Impedance Measurement ASIC

The Impedance measurement module is composed of a sine wave oscillator which generates a rail-to-rail signal. This output is fed into an on-chip attenuator which subsequently alters the amplitude of this signal to a magnitude appropriate for impedance spectroscopy. The design routes the intermediary inputs and output to chip pads, where they may either be connected using external "jumpers" (as described above) . If there is signal corruption at any stage, the input to the next stage can alternatively be provided from an external source, thus maintaining the ability for perform impedance measurements in spite of sub-circuit dysfunction. This scheme is summarized in Figure 3.10 below.

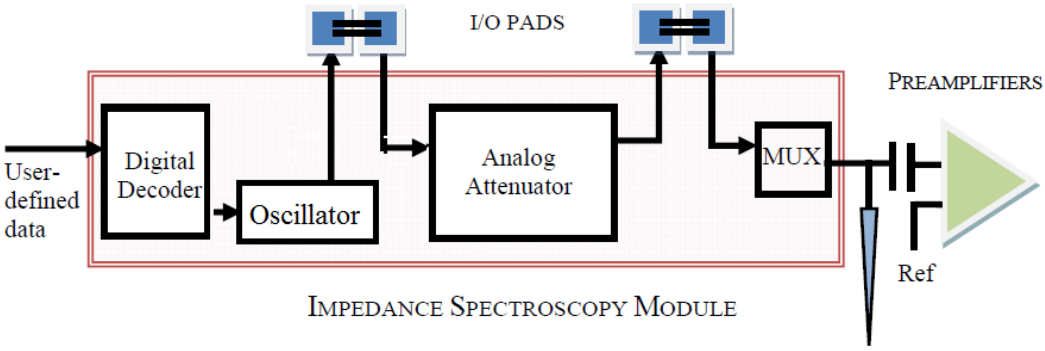


Figure 3.6: Impedance Measurement Module.

3.4.1 Implementation of a Sinusoidal Oscillator

An oscillator is an electronic circuit that is able to produce AC signals without any external inputs. This is achieved by deliberately creating a persistent but predictable and controlled instability in a feedback system. A feedback system, depicted in Figure 3.11 is characterized by its forward gain A and its feedback quotient β.

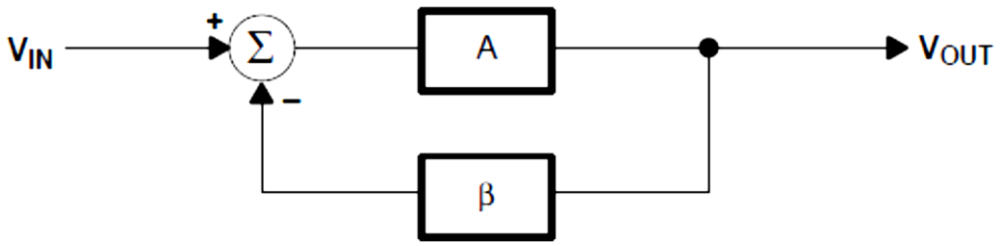


Figure 3.7: A canonical model of a Feedback system

The overall transfer function of this system is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1+A\beta} \tag{3.3}$$

An unstable feedback system is one that is unable to satisfy its transfer function. In the example above, this happens when the denominator of the transfer function equals zero, given by $A\beta = -1$. This condition, known as Barkhausen's criteria, is the fundamental requirement for forcing a circuit into oscillation, and requires that the loop gain be 1 and the phase shift be -180° [43]. When this occurs, the output heads to infinity, constrained only by power supply. If the system is composed of active elements, A dynamically changes its value to steer $A\beta$ away from singularity by slowing and eventually halting its trajectory. If the system is designed to maintain linearity, this causes the output to reverse direction and head toward the opposite rail. This continues cyclically as long as a closed loop gain of one is maintained. A loop gain greater than 1 creates an incremental growth in oscillatory amplitude leading to eventual saturation, while a gain less than one leads to dampening of the oscillation amplitude.

Feedback circuits employing RC elements for frequency tuning in combination with operational amplifiers for gain control have been a standard engineering approach for integrated oscillator design at frequencies less than 1 MHz

[43, 44]. They offer several advantages including low power consumption and simple implementation with a few on-chip components. An oscillator may be designed to provide square or sinusoidal signals, where the latter is accomplished by adding specific circuit components for pulse-shaping.

The Wien Bridge Oscillator, demonstrated in Figure 3.8, is a popular sinusoidal oscillator design due to its simplicity and ease of implementation. It utilizes an opamp with high GBW to provide dynamic forward gain, and a combination of positive and negative feedback (with the positive slightly outweighing the negative) to achieve stable oscillations. Lead and lag RC networks are used in the positive feedback pathway to introduce the phase shift, while the negative feedback is achieved via resistors. Figure 3.8 also demonstrates the use of automatic gain control (AGC) elements which reduce signal distortion close to power rails. The use of non-linear elements such as diodes in the AGC allows for selectively reducing the gain of the negative feedback close to the power-rails, allowing for pulse shaping.

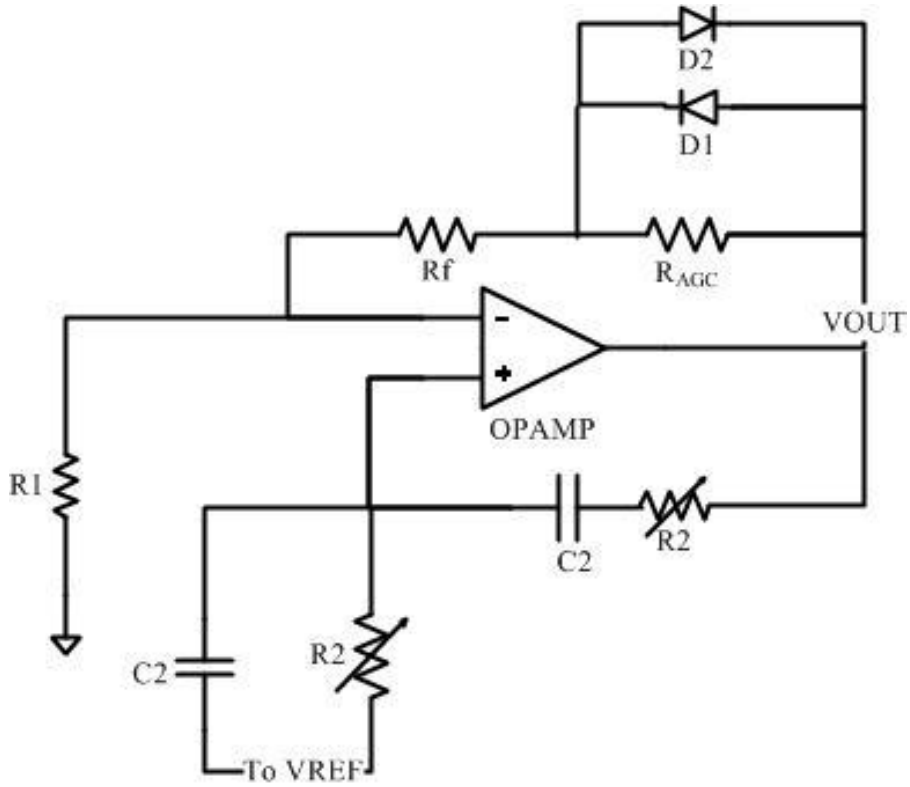


Figure 3.8: Wien Bridge Oscillator

A Wien Bridge uses an inverting amplifier with a forward gain A given by:

$$\frac{V_{out}}{V+} = 1 + \frac{R_f + R_{AGC}}{R_1} \tag{3.4}$$

The feedback gain β is given by:

$$V_+ \; V_{out} * \left(\frac{Z_{R2||C2}}{Z_{R2||C2} + Z_{R2+C2}}\right) \tag{3.5}$$

where $Z_{R2||C2}$ is the complex impedance of the parallel combination of C2 and R2 and Z_{R2+C2} is the impedance of the series combination of R2 and C2. This gives

$$\beta = \frac{V_+}{V_{out}} = \left(\frac{1}{3 + j\omega R_2 C_2 + 1/j\omega R_2 C_2}\right) \tag{3.6}$$

Barkhausen's criteria for this circuit is satisfied when Aβ = -1 , or

$$\left(\frac{1}{3+j\omega R_2 C_2+\frac{1}{j\omega R_2 C_2}}\right)\left(1+\frac{R_F+R_{AGC}}{R_1}\right) = -1$$

This occurs at $R_2C_2 = \frac{1}{\omega R_2 C_2}$, making the circuit oscillate with the characteristic frequency f_0 which is given by:

$$f_0 = \frac{1}{2\pi R_2 C_2} \tag{3.7}$$

The unity gain requirement at the resonant frequency is met by sizing the forward gain elements appropriately to offset the feedback gain. Since β = 1/3 at f0, A is set to be 3, which gives a 2:1 ratio of feedback resistors. The Automatic gain control is selected such that the forward gain may in drop down to sufficiently less than 3 close to the supply rails to prevent saturation and maintain pulse shape.

3.4.2 Design of a Tunable Wien Bridge Oscillator

Neural electrode impedance measurements have historically been made at 1 kHz. While this has been useful in tracking the electrode interface, it only yields point data. We hypothesized that data across a range of frequencies would offer greater insight into the complex mechanisms at play at the electrode-tissue interface. Since signal frequencies of interest in broad-band neural data span 1 Hz – 8 kHz, a logarithmic Wien Bridge Oscillator with 5-bit control from 1 Hz to 10 kHz is chosen to be implemented.

The oscillator comprises a 2-stage CMOS opamp designed for high gain-bandwidth product. The AC response of the opamp is shown in Figure 3.9

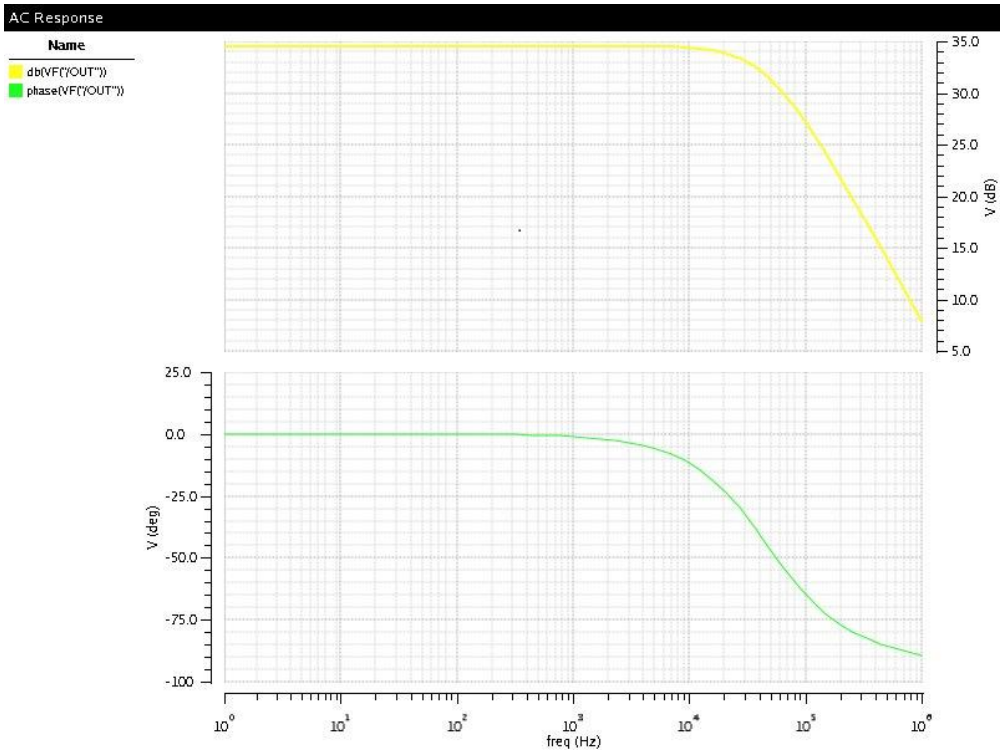


Figure 3.9: AC response of 2-stage operational amplifier used in Wien Bridge Oscillator

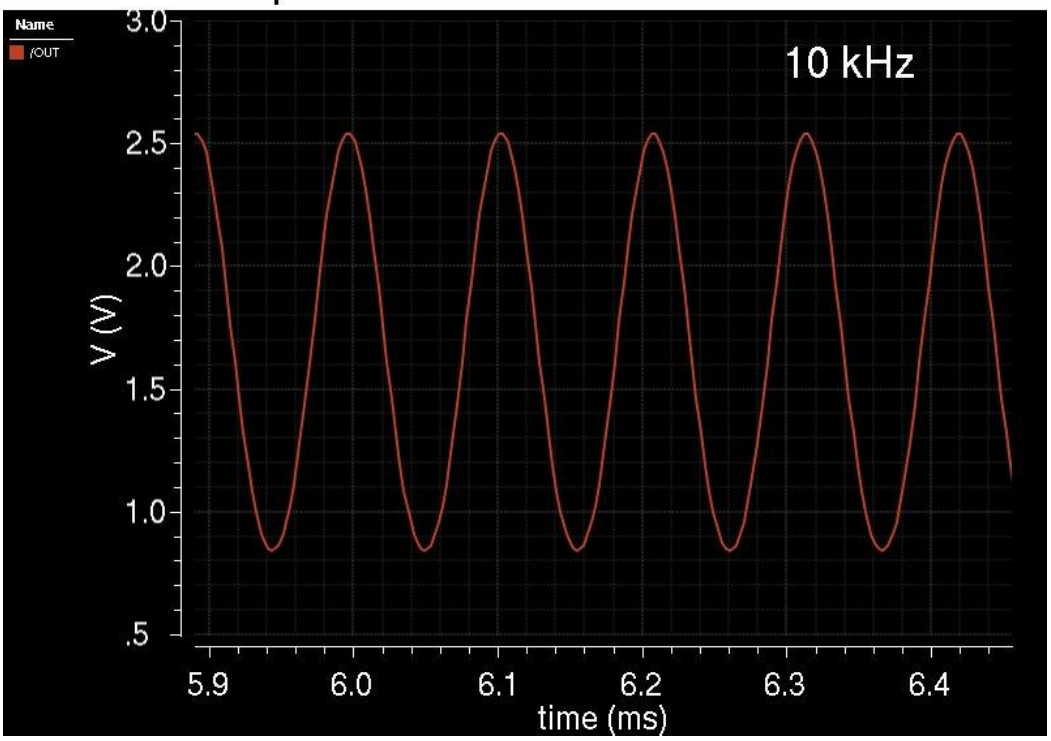
The forward gain elements are sized at $R_f = 24$ kΩ (implemented as two 12 kΩ resistors in series) and $R_1 = 12$ kΩ. The Automatic gain control mechanism uses an additional 24 kΩ resistor in series with a diode. This combination is activated in parallel with one of the 12kΩ components of R_f to drop the total R_f to 20 kΩ when the voltage across the diode exceeds the forward-junction voltage (~ 0.7V). The reduction in gain then allows for the appropriate sinusoidal pulse shape to form at the output.

Tunable frequency is achieved through a combination of fixed off-chip capacitor and 5 distinct on-chip resistors. This allows for minimization of chip area. In our current implementation, a 100 nF capacitor is used. The circuit may be driven

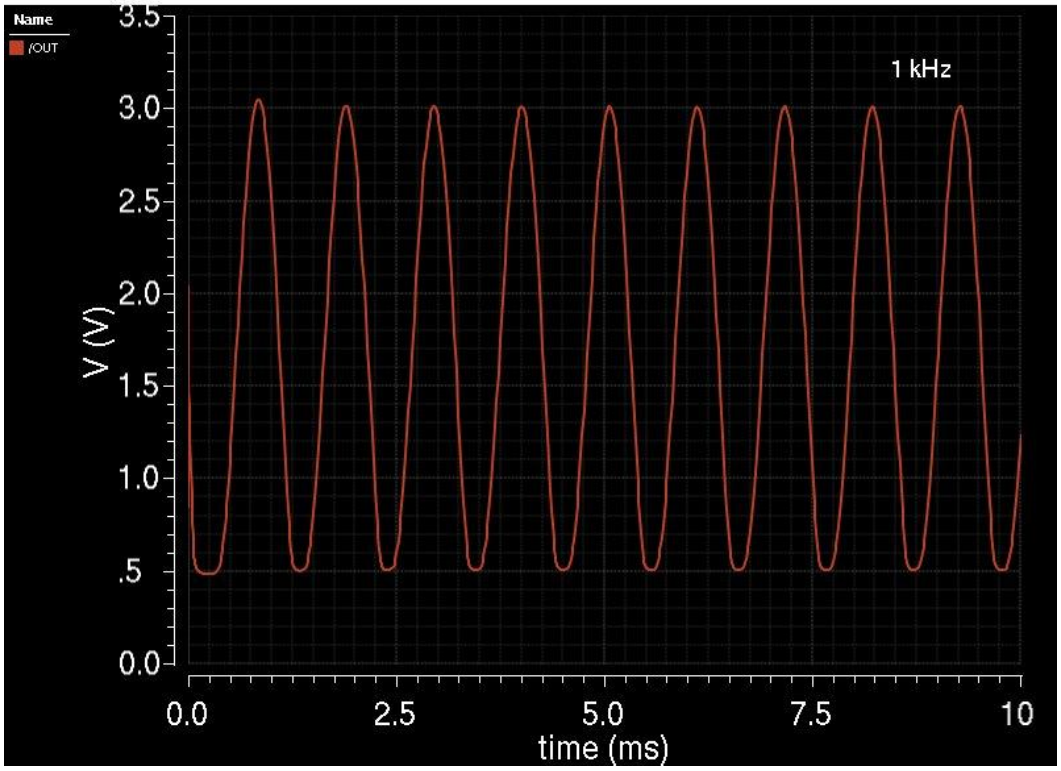
with +/- 1.65 V split supplies, or a 3.1 V single-ended supply by externally setting a bias on the mid-rail voltage. It yields rail-to-rail sinusoidal signals at 1 Hz, 10 Hz, 100 Hz and 1 kHz with low distortion. The 10 kHz sinusoidal is slightly gain-limited and only approaches ~ 50% of the full voltage swing. Figure 3.10 shows transient simulations of the oscillator across the range of operation:

The RC feedback elements in the bandpass essentially form a bandpass filter selecting for the resonant frequency. The AC simulation of the oscillator, shown in Figure 3.11 demonstrates the resonant transfer function of the circuit at each of the frequencies of operation:

Transient Response



Transient Response



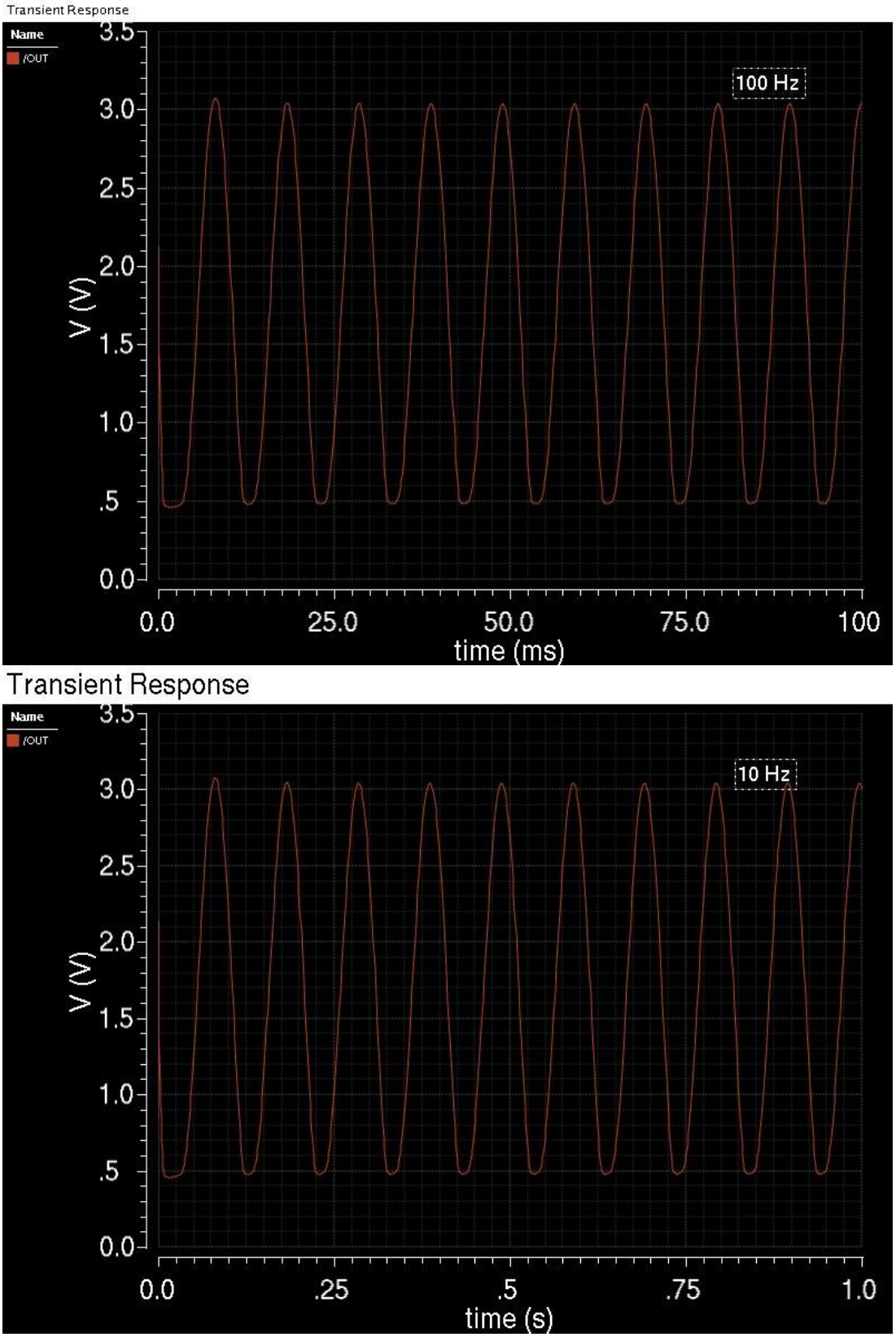


Figure 3.10: Transient simulations of Wien Bridge Oscillator across the full range of operation

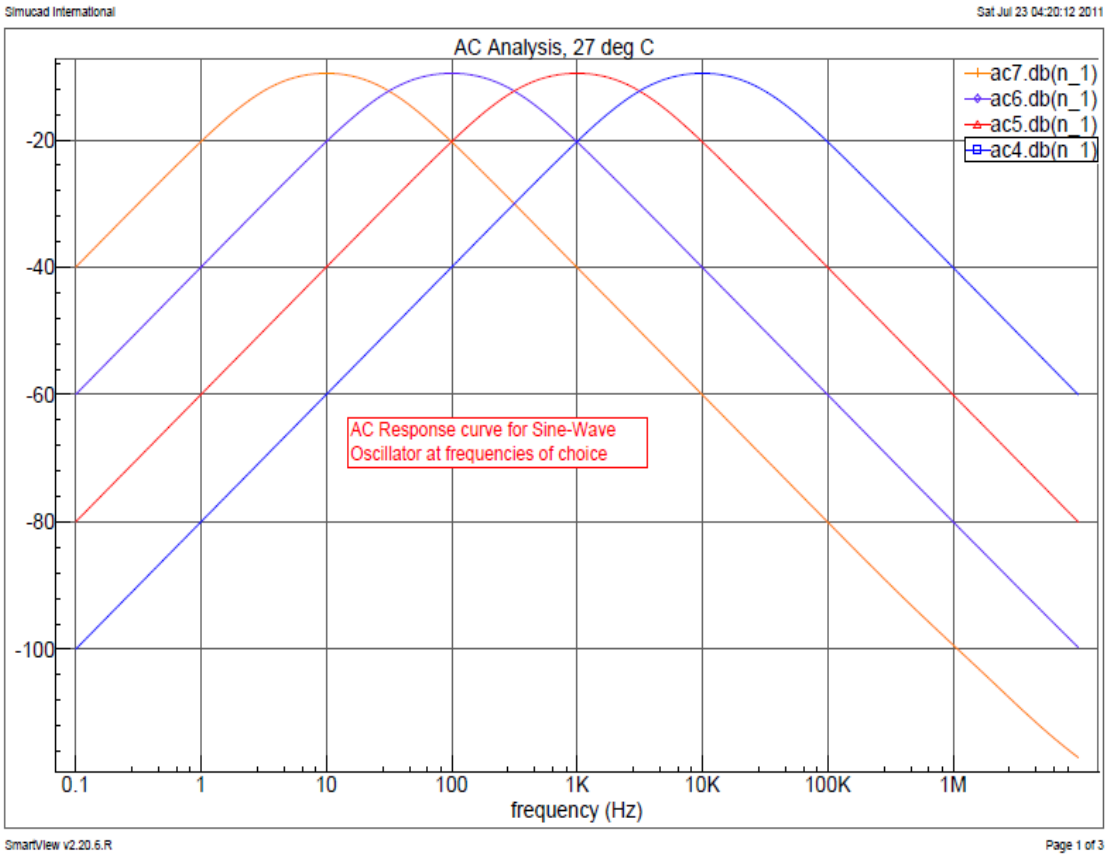


Figure 3.11: AC response of the Wien Bridge, showing a stable loop gain at each frequency

The Wien Bridge Oscillator was designed and fabricated in the ON-SEMI 0.5 µm CMOS technology. It was integrated with the 16-channel amplifier chip described in Chapter 3. The frequency control signals were supplied as a serial input to a digital controller block on-chip. This was described in hardware-description language and synthesized using Mentor Graphics Leonardo Spectrum™. The detailed function of the controller block is described in the context of stimulation in Chapter 5. For the purposes of impedance measurements, the controller enables the Wien bridge oscillator, provides the appropriate frequency selection and routes the oscillator output to the appropriate electrode site (the address of the site is part of the serial input).

Oscillator Layout is shown in Figure 3.12. It occupied 300 µm x 300 µm of space and consumes 460 µA from a 3.1V supply.

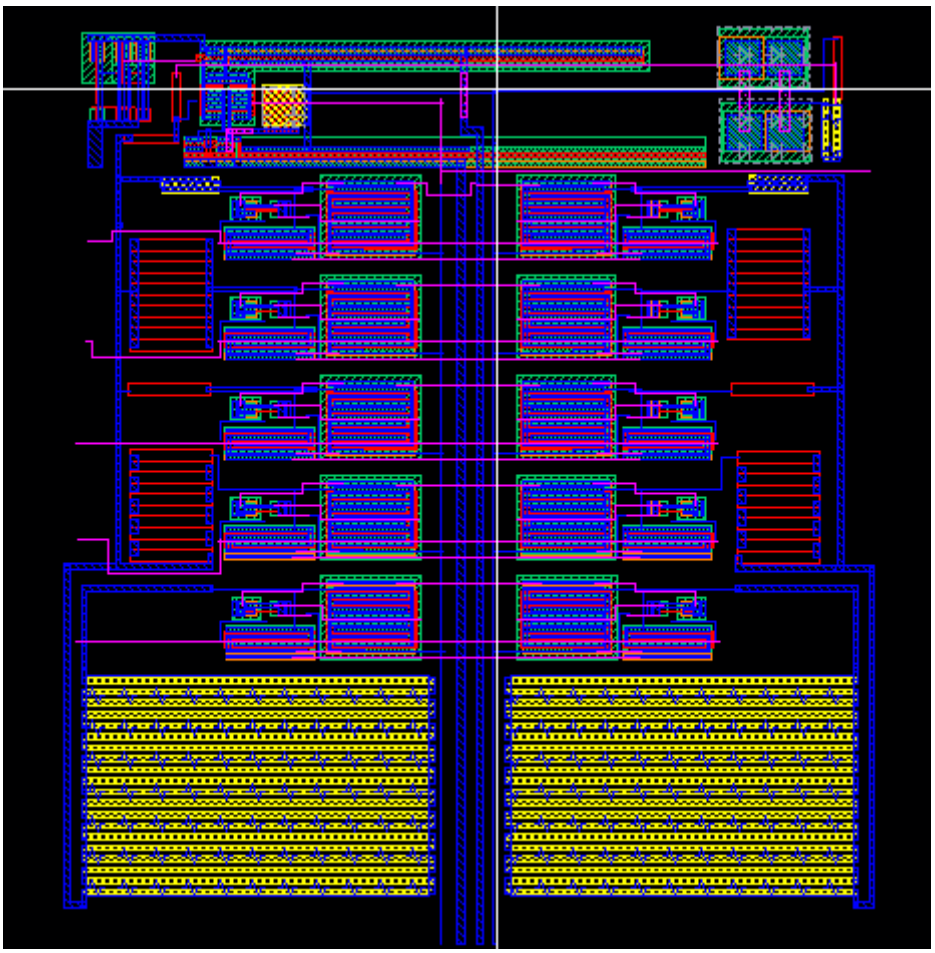


Figure 3.12: Layout of the Tunable Wien Bridge Oscillator

The post-fabrication testing of the Wein bridge showed significant signal distortion. This was thought to be associated with the deviation of the behavior of the gain control elements from simulation models. Circuit gain is also very sensitive to mismatch in resistor sizing, and difficult to design for run-to-run robustness. The decision was thus made to implement a full impedance spectroscopy functionality instead of a few finite probe frequencies in the next generation by utilizing a digital approach for square wave generation. The description of this Impedance Spectroscopy ASIC is described in the next section.

3.5 Impedance Spectroscopy using a Square Wave Generator

Impedance spectroscopy is classically known as a technique using well-known sinusoidal excitation sources. The successful use of square wave voltage sources has however been recently reported in literature in widespread disciplines from battery engineering to bioimpedance monitoring [45-47]. This is an enticing prospect for BCI applications because it may be implemented digitally. This would allow for a compact, tunable signal source which can easily be integrated onto the same ASIC platform. Furthermore, it would take away the overhead and uncertainly associated with designing tuned analog circuitry.

Impedance measurement circuits for BCIs rely on the ability of the neural signal amplifiers to also accurately record the impedance response of electrodes. Verifying that the amplifier's performance, particularly slew rate, is compatible with recording the impedance source waveforms is an important preliminary task. Figure 3.163shows the outcome of this test for our neural amplifier design.

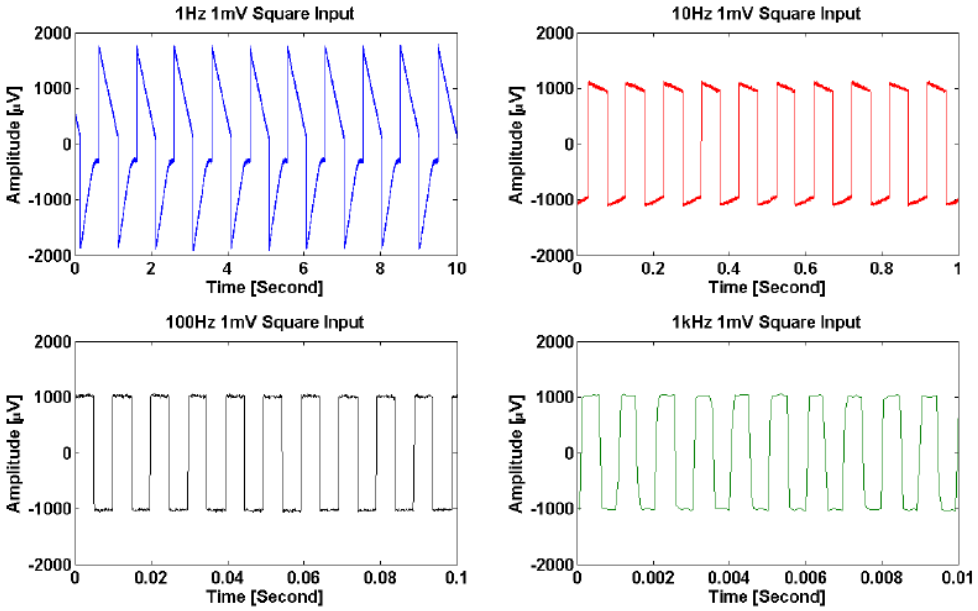


Figure 3.13: Neural Amplifier Response to square pulses from 1 Hz to 1 kHz. 1 Hz data demonstrates the effects of the DC filtering high-pass with a cutoff at 1 Hz

This data was obtained by setting up a benchtop test for neural recording amplifiers. 100 kΩ resistors were used to model the microelectrodes. A 1 mV square wave from a bench top pulse generator was then applied to the amplifiers through the dummy electrodes, and the output response was characterized for a range of frequencies between 1 Hz and 1 kHz. The signal distortion at the low-end of the frequency spectrum may be mitigated by selecting the (tunable) high-pass cutoff frequency to be lower than the frequency of interest for impedance spectroscopy. Similar distortion is seen at 10 kHz (data not shown) due to the 7.8 kHz low-pass cutoff for the amplifiers, but this is outside the frequency range of interest, and is therefore not a concern.

3.5.1 System Architecture:

The overall architecture of the square-wave impedance spectroscopy system is identical to that described for the Wien bridge oscillator based approach with the exception that the sinusoidal source generator circuit is absorbed into the digital controller block, which is able to take in a serial data stream with the impedance spectroscopy parameters and provide a TTL level square wave of the desired frequency. This is subsequently divided using an on-chip resistive divider circuit and a fed through a unity gain buffer to reduce its output impedance. Multiplexing circuitry is implemented to direct the impedance signal to a specific channel in the amplifier array. This is demonstrated in Figure 3.14. Of note, this prototype system is integrated with a 100-channel amplifier ASIC.

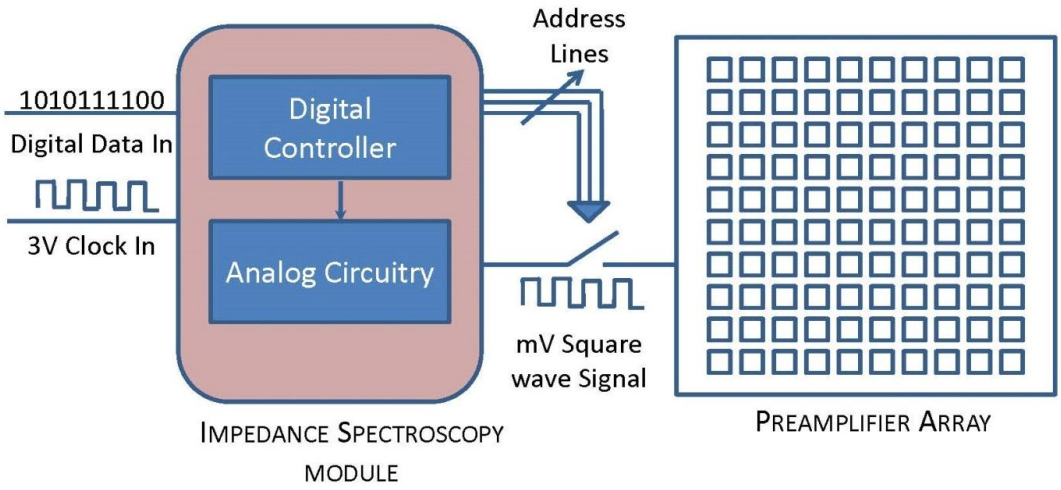


Figure 3.14: System architecture for 100-channel impedance spectroscopy ASIC

The individual components of this system are described in detail below:

3.5.2 Digital Controller

This is a crucial component of the system since it acts as the serial input interface, the square wave generator and the signal multiplexing decoder. Serial data is delivered in a 44-bit packet with a structure described in Table 3.1

8 bit	SYNCH	Packet Start Identifier
1 bit	PARITY	Parity Check (Even)
3 bit	MODE	000 Record 001 Nominal Impedance 111 Impedance sweep
8 bit	ADDRESS	Electrode Address
16 bit	FREQUENCY	Square Wave Frequency
8 bit	**SYNCH**	**Packet End Identifier**

Table 3.1: Packet Structure for Serial data to the Impedance Spectroscopy ASIC

There are 3 important parts to the data packet.

i. *Address bits*: These determine which channel the spectroscopy signal is directed to. Additionally, there is a mechanism to allow parallel distribution of the impedance source signal to all channels by setting all 8 address bit to 1 (decimal 256).

ii. *Mode bits*: These may be set to record, impedance or sweep (as described above). In the nominal impedance mode, a single source frequency is generated. The maximum frequency that is possible to generate is ½ the clock provided to the controller. The sweep mode, on the other hand, generates a frequency sweep by sequentially generating signals of increasing frequencies (for 10 signal cycles each). The upper bound for the sweep is always the highest possible frequency (1/2 clock) while the lower bound is set by the value of the frequency bits in the data packet.

While exclusive recording is a mode that may be selected via the digital controller, the system is designed such that this is the default mode of operation. The system is able to record in the absence of any serial data input and even if the digital controller module is left powered off.

iii. Frequency bits: These do exactly what their name suggests. The actual implemental waits the number of cycles indicated by these bits before toggling the state of the output signal. This means that the effective transfer function of 16bFrequency to output signal frequency is:

$$f_{output} = \frac{f_{CLK}}{2*(16bitFreq+1)} \quad (3.8)$$

For example, if the f_{clk} = 20 kHz and 16bitFreq = 3, $f_{output} = f_{clk}/8$ = 2.5 kHz.

The digital controller was developed as VHDL (VHSIC Hardware Description Language) using Active HDL Software. Once the digital decoder had been designed and verified through simulation, it was converted into transistor level layout by Mentor Graphics Leonardo Spectrum Synthesis tool. The design was optimized for area so as to minimize the overall footprint of the Impedance Spectroscopy ASIC. Total chip area is an important constraint since the 100-channel ASIC must remain compatible with direct integration approaches such as flip-chip bonding to the 4 mm x 4 mm 100-channel Utah MEA. The top level layout of the controller is shown in Figure 3.15 while Figure 3.16 demonstrates the post-synthesis layout simulation.

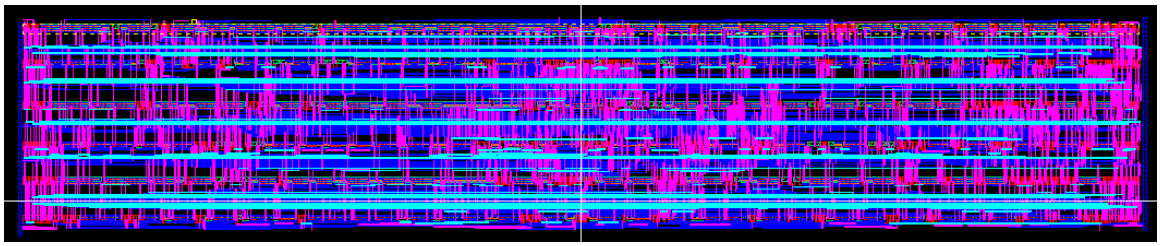


Figure 3.15: shows the synthesized layout of the digital decoder sub-circuit.

Controller output frequencies as a function of digital input code were analyzed across the range of operation and are demonstrated in Figure 3.17.

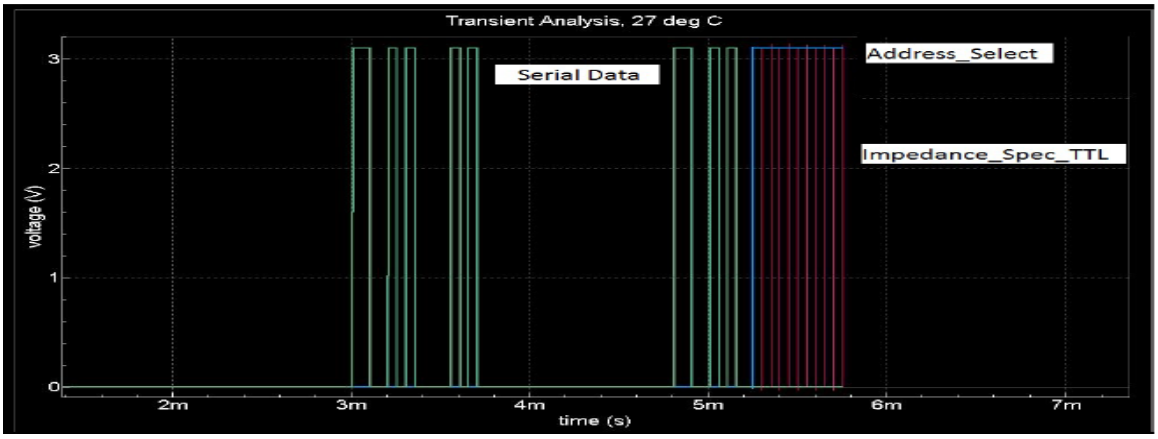


Figure 3.16: Simulation data from digital decoder. The data packet is set to a mode of '001', an address of 64 '0100 0000' and a 16bFreq of 0 '0000 0000 0000 0000'. Clk is set at 20 kHz. The blue waveform demonstrates the toggled address line and the pink waveform demonstrates a 10 kHz square wave as expected.

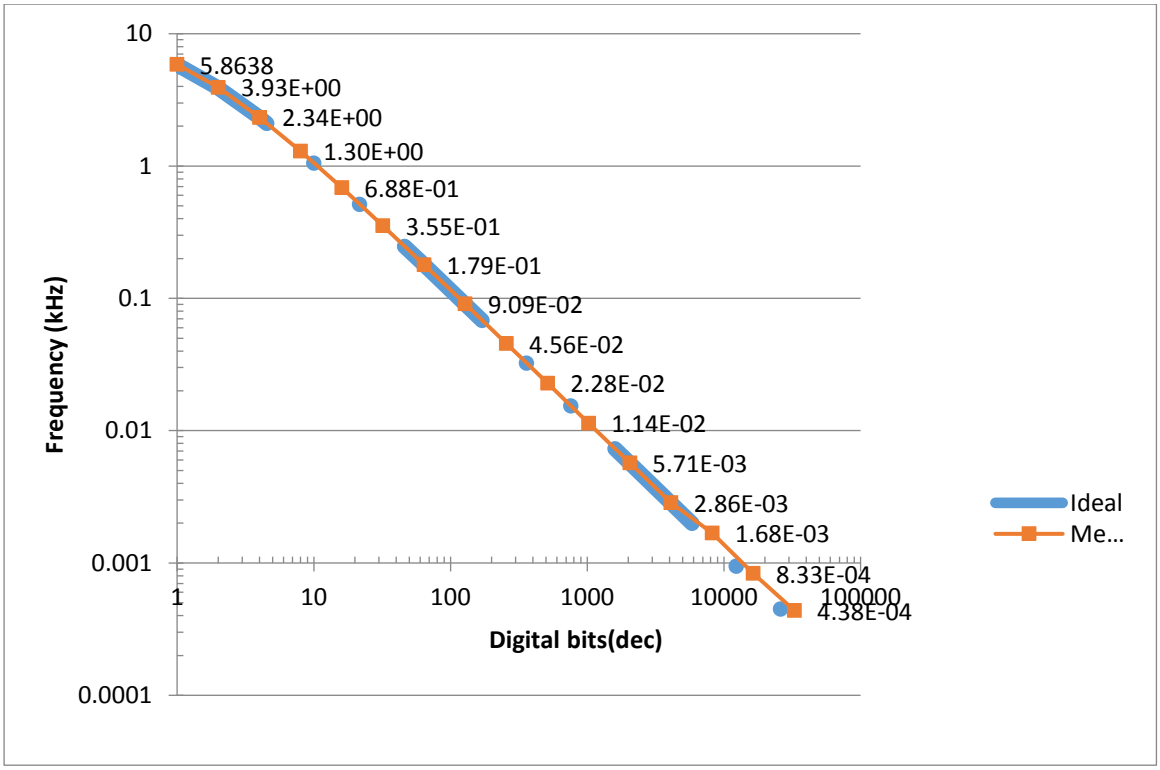


Figure 3.17: Controller Frequency Output Versus Digital code. Calculated values are compared with Measured values to confirm Controller Frequency transfer function.

3.5.3 Analog Attenuator

The purpose of the analog circuitry on the Impedance Spectroscopy ASIC is to attenuate the square wave generated by the Digital controller module. This is achieved by a 1:500 on-chip resistive divider. The latter produces a ~ 6mV signal (depending on VDD to the controller). The output of the divider is the buffered with a 2 stage CMOS opamp configured as a follower. The low output impedance of the opamp output stage allows for reliable application of the generated signal to the external test impedance. Figure 3.18 depicts the overall system diagram while Figure 3.22 shows the analog attenuator layout. It is important to note that the output of the analog attenuator goes through a second resistor $R_{divider}$. This forms one half of a second resistive divider, while the other half is the test Impedance Z_{ext}. The input node of the amplifier senses the voltage at the node between the elements of the second divider, thus assessing the ratio of these 2 elements. The sense-amplifier input node voltage is given by 3.9:

$$V_{in} = \frac{Z_{ext}}{R_{divider}+Z_{ext}} \tag{3.9}$$

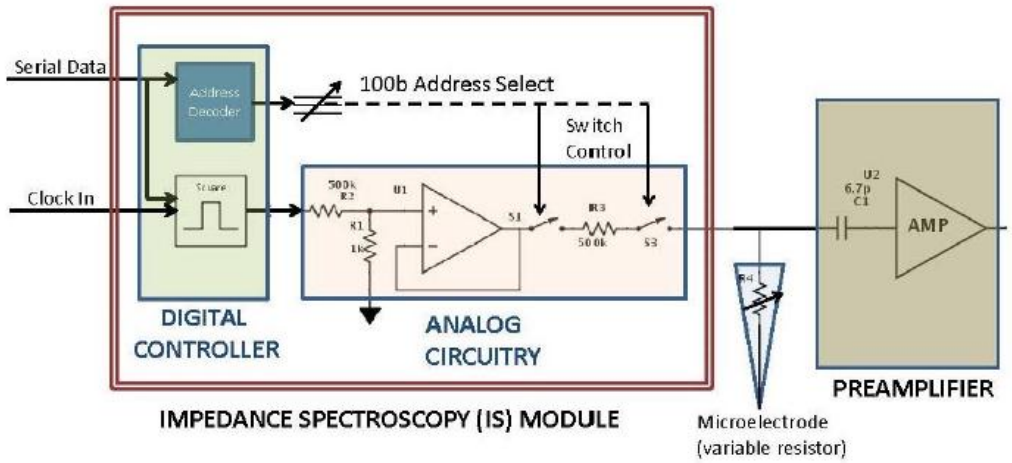


Figure 3.18: Schematic of the impedance Spectroscopy ASIC, highlight the Analog Attenuator.

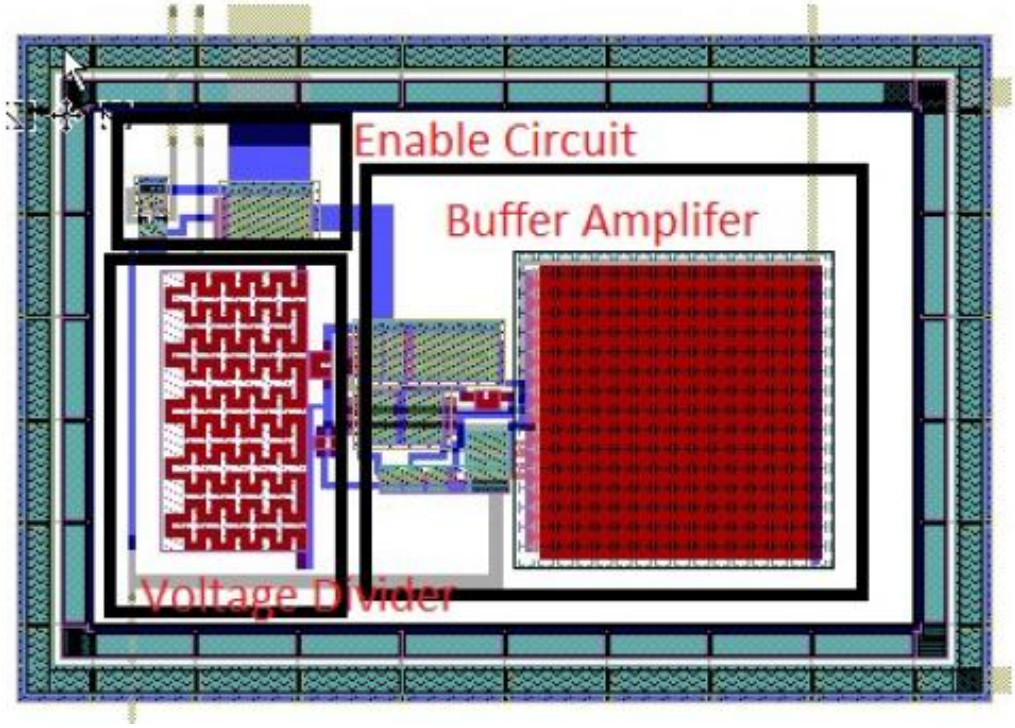


Figure 3.19 Layout of the Analog Attenuator. A guard rail is implemented to protect this analog circuitry from noise generated in the adjacent digital blocks.

CMOS Opamp Buffer

The design of the CMOS operational amplifier is crucial to the proper functioning of the impedance module. The buffer amplifier is implemented as a standard 9-transistor 2-stage opamp. It is self-biased and designed to for a gain-bandwidth product > 1MHz. Figure 3.20 shows the schematic of the buffer amplifier. The AC response of the opamp is demonstrated in Figure 3.21

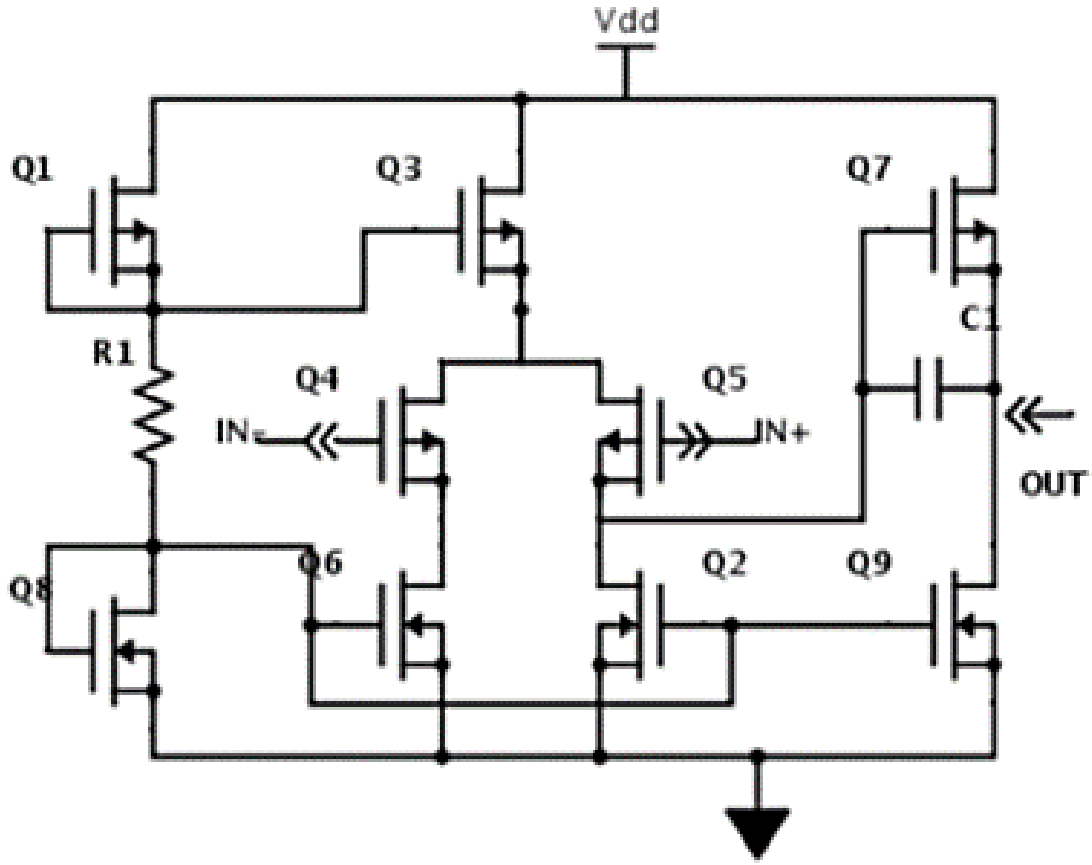


Figure 3.20: Schematic of 2-stage CMOS opamp used as a unity gain follower

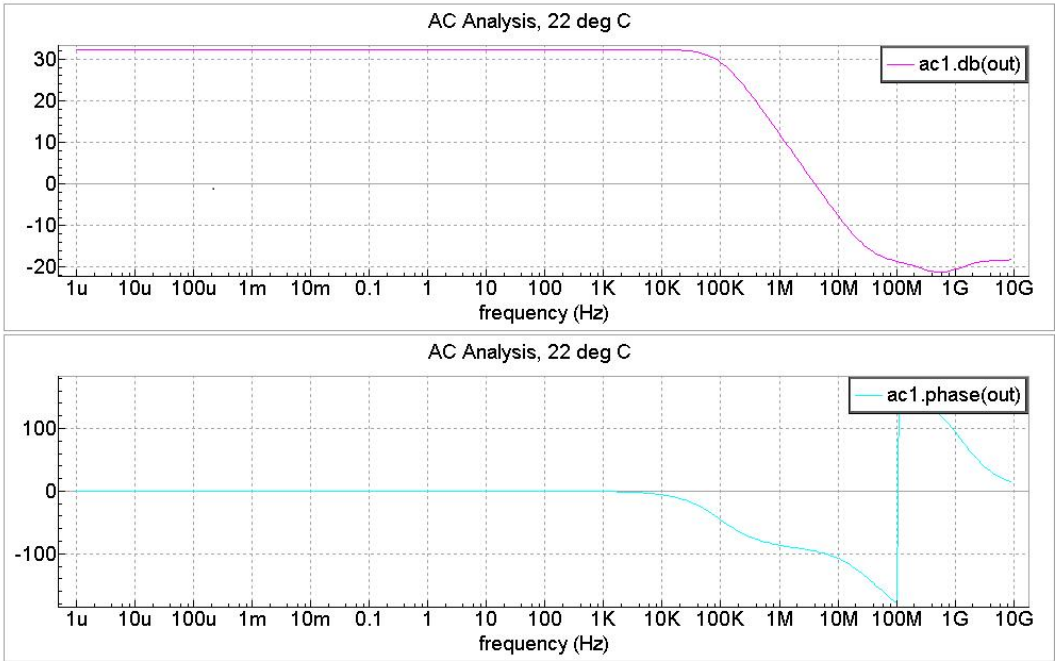


Figure 3.21: AC response of the CMOS opamp. The -3dB frequency is at 100 kHz

The operation of the analog attenuator is shown in Figure 3.22.

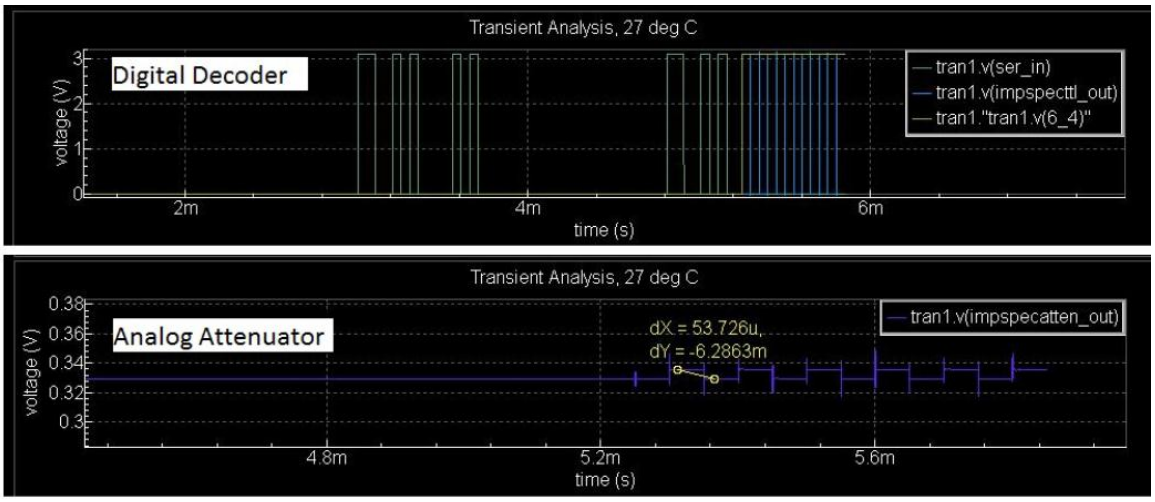


Figure 3.22: Analog Attenuator Output. The top frame shows the digital decoder and its generation of a TTL square wave. The bottom frame shows the output from the attenuator, with a square wave of the same frequency, but smaller in voltage magnitude (6 mV).

3.5.4 Integration with 100-channel Preamplifier Array

The Impedance Spectroscopy module was integrated with the existing 100-channel amplifier array once its performance was verified with post-layout simulations. The top level circuit layout is shown in Figure 3.23 with the impedance spectroscopy module adjacent to the 10 x 10 grid of recording amplifiers. One of the most important things to verify at this top level is the maintenance of the recording capability of the amplifiers after the addition of the impedance spectroscopy circuitry. Figure 3.24 demonstrates the operation of the amplifiers when presented with sinusoidal waveforms of various different frequencies.

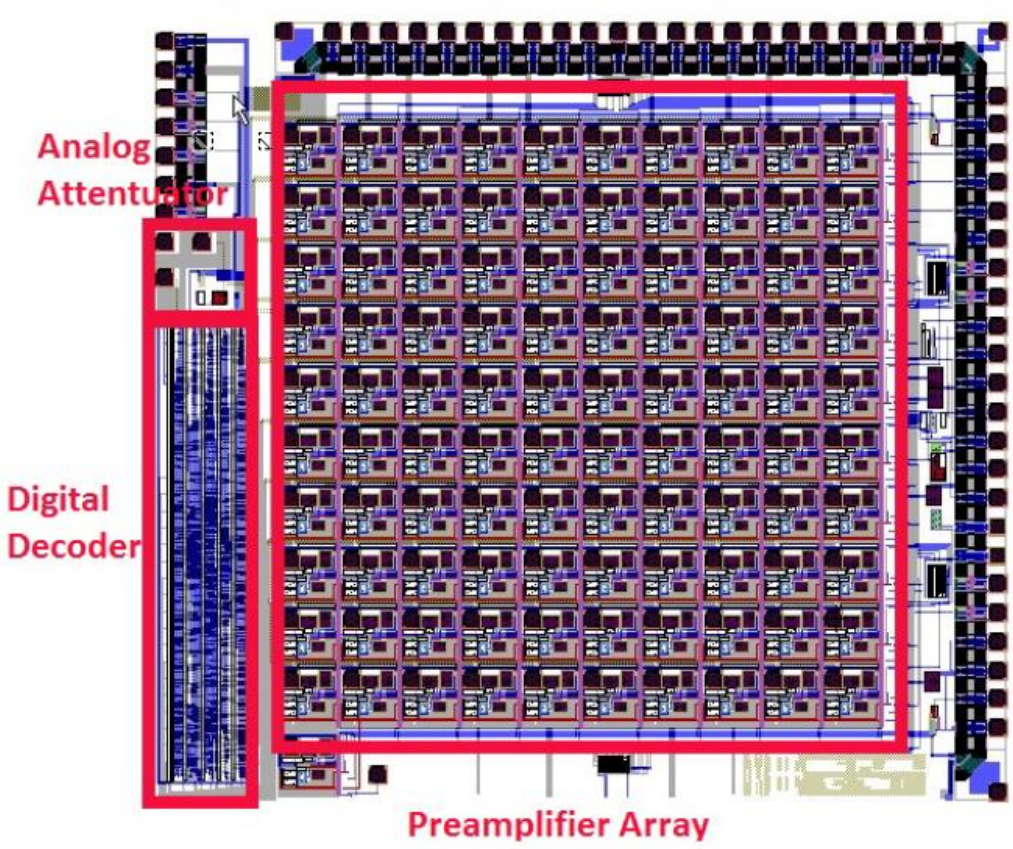


Figure 3.23: Top level Impedance Spectroscopy Chip Layout. The IS module layout is added to the periphery of the preamp array.

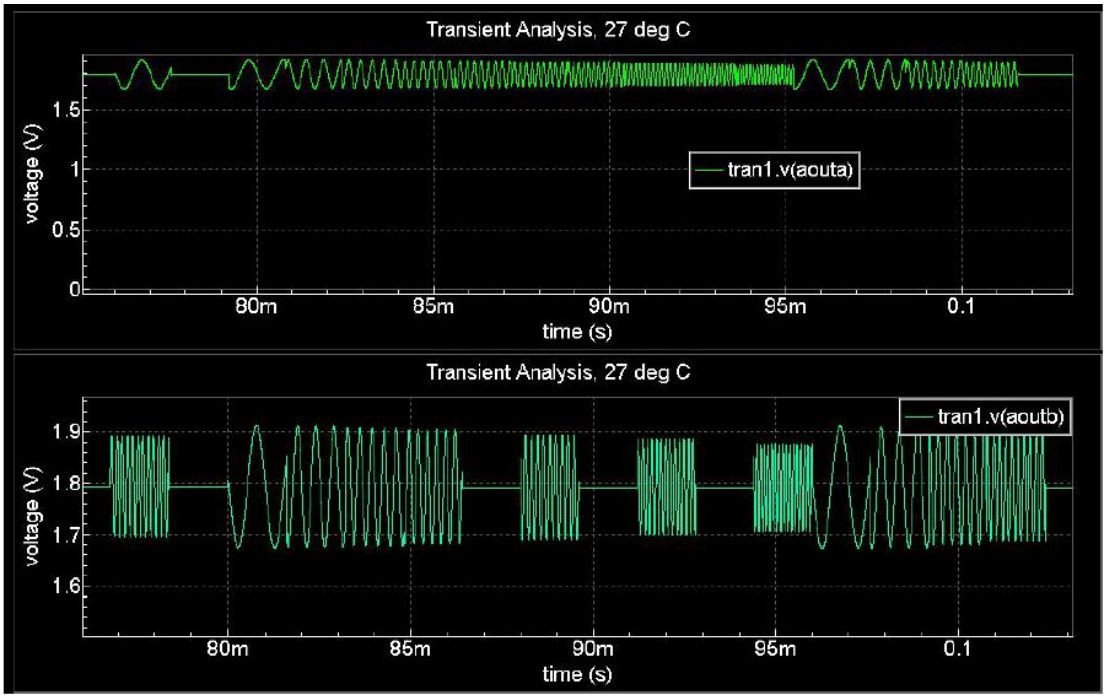


Figure 3.24: Recording function of the preamplifiers. Each trace shows the multiplexed output from 1 bank of 50 amplifiers. Sinusoidal waveforms with frequencies from 1 – 5 kHz were used. Sampling clock was set at 160 Hz for improved visualization.

The top-level functionality of the impedance spectroscopy module was verified, as demonstrated by Figure 3.25. For full operation of the module, the digital controller and the analog attenuator must produce 3V and 6 mV square waveforms respectively. The frequency of the signals must match that determined by equation 3.8. The attenuated signal is then applied to a test impedance and must produce a further attenuated signal at the amplifier input node. For a 100 kΩ external impedance in this test case, this value is 1mV (based on the 2nd divider ratio of Z_{ext} /500 kΩ + Z_{ext}).

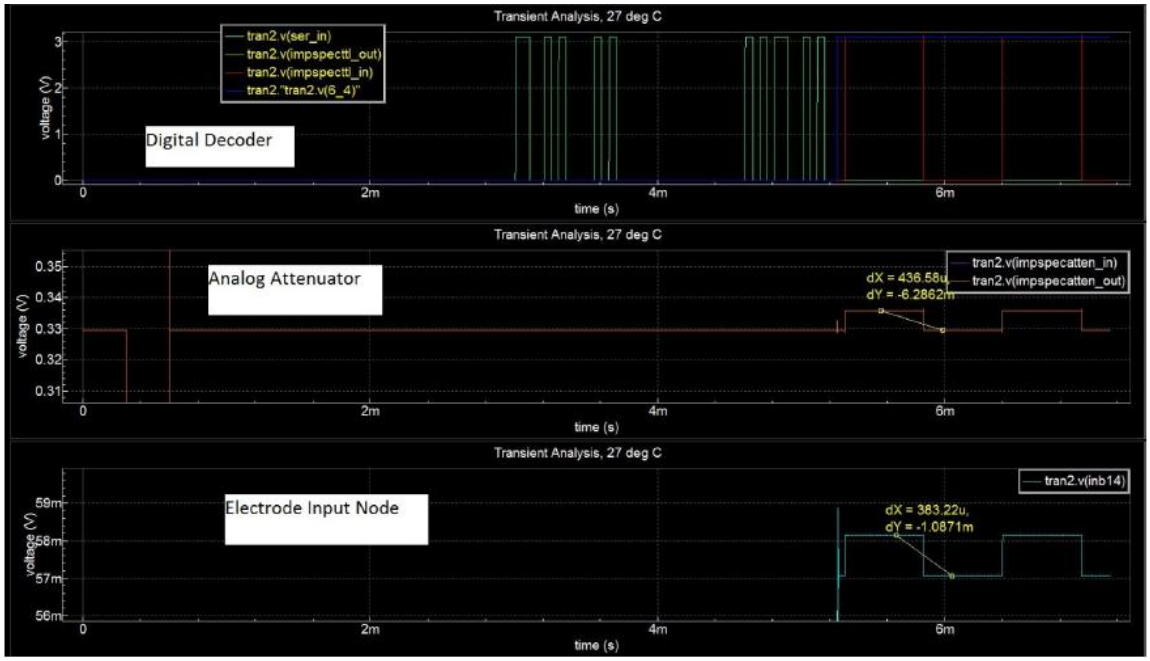


Figure 3.25: Impedance Spectroscopy module (after integration with 100-channel Preamplifier array)

The impedance spectroscopy module was designed with a safety override function in order to have the capability to turn the system off in case of an emergency. Figure 3.26 demonstrates use of this function. The reset signal must be asserted in order for the module to function; turning this signal off emergently shuts down the module and turns off its power supply until the signal is reasserted. This makes the chip revert back to recording mode as described earlier.

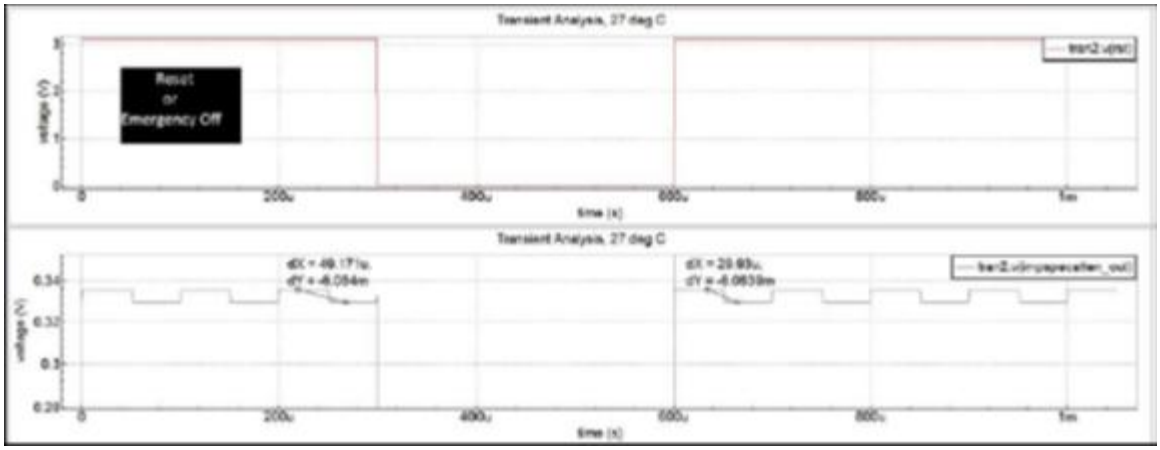


Figure 3.26: Emergency Shutdown through reset. The system is functional as demonstrated by the 6mV square wave signal output from the analog attenuator. When reset is deasserted, output turns off. System functionality returns when reset is turned on again.

3.5.5 Layout Considerations

The impedance spectroscopy module is composed of both analog and digital parts. The latter has an active clock which can compromise the performance of the analog counterparts. When laying out the circuitry, special care and attention was invested in ensuring that the analog and digital parts were isolated as much as possible. Separate and dedicated power supply pads were created for each sub-circuit.

Fast-switching traces such as the clock line were routed distant to analog signals to prevent cross-coupling. When separation of the traces was not possible, the analog traces were routed on metal1 with a ground plane on metal2. The digital lines were then routed in metal 3 to provide shielding to the analog signals. The analog attenuator was enclosed in a guard rail for further protection from digital noise. Extra care was taken to reduce parasitics by minimizing trace lengths and layer to layer cross-overs and the path length from the smallest attenuated signal (1mV) to the electrode was minimized by placing the second resistive divider adjacent to the electrode bond pad.

3.6.6 Fabrication and Testing

The ASIC was designed and fabricated in ON-SEMI 0.5 μm CMOS. Figure 3.27 shows a photomicrograph of the fabricated chip.

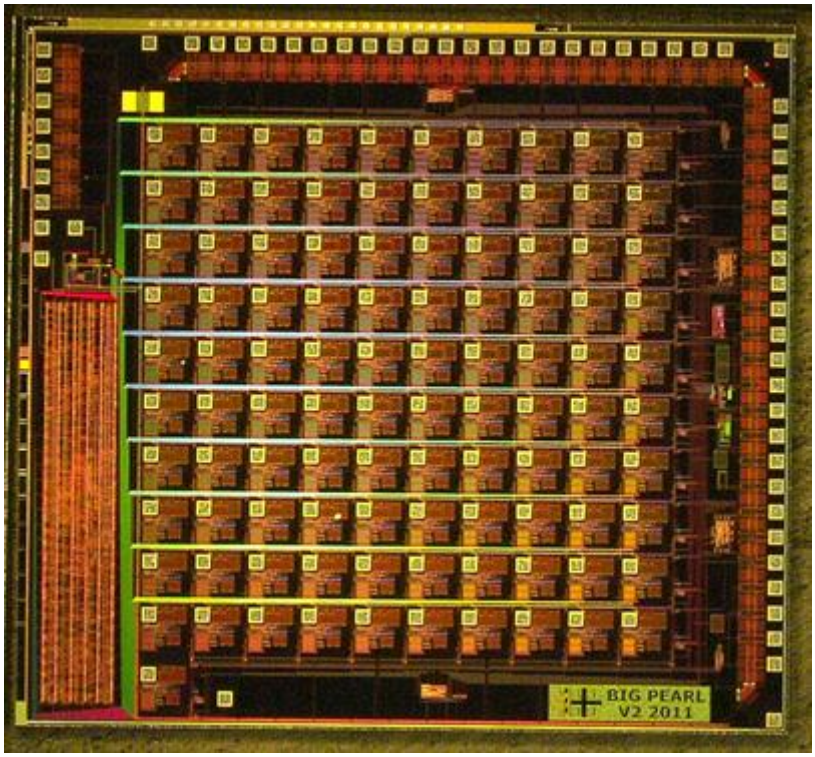


Figure 3.27: Photomicrograph of 100-channel Impedance Spectroscopy ASIC

A testing matrix was developed for benchtop characterization and subsequent systems-level testing. Results from bench top testing of 40-pin DIP packaged device are described below while development and testing of an impedance spectroscopy system for in vitro and in-vivo experiments is discussed in Chapter 4.

i. *Recording function without impedance spectroscopy powered:*

This is the baseline operation mode of the 100-channel amplifier chip, and is basic verification test to ensure that the add-on circuit has not created any performance problems for the amplifiers. Figure 3.28 shows recording amplifier output in response to an external sine wave applied to its input node.

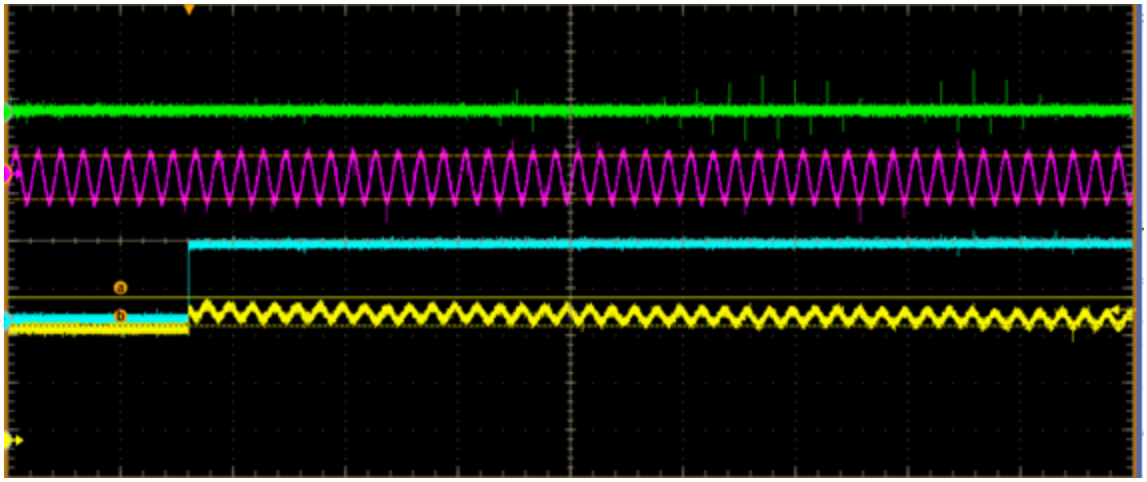


Figure 3.28: Amplifier Recording performance. The pink waveform shows a sine wave source which is applied to the amplifier input. The blue waveform is the channel addressing clock, while the yellow waveform shows the amplifier output, sampled at the multiplexor output

ii. *Recording tests with Impedance Spectroscopy module turned on:* This allows for characterization of any cross-talk or added noise due to the presence of the impedance spectroscopy module. The extensive characterization of this mode is not possible in a bread-boarded bench top setup since it requires noise analysis best performed with an optimized systems approach. Figure 3.29 however, demonstrates the lack of any obvious difference in recording performance before and after turning on the impedance spectroscopy signal.

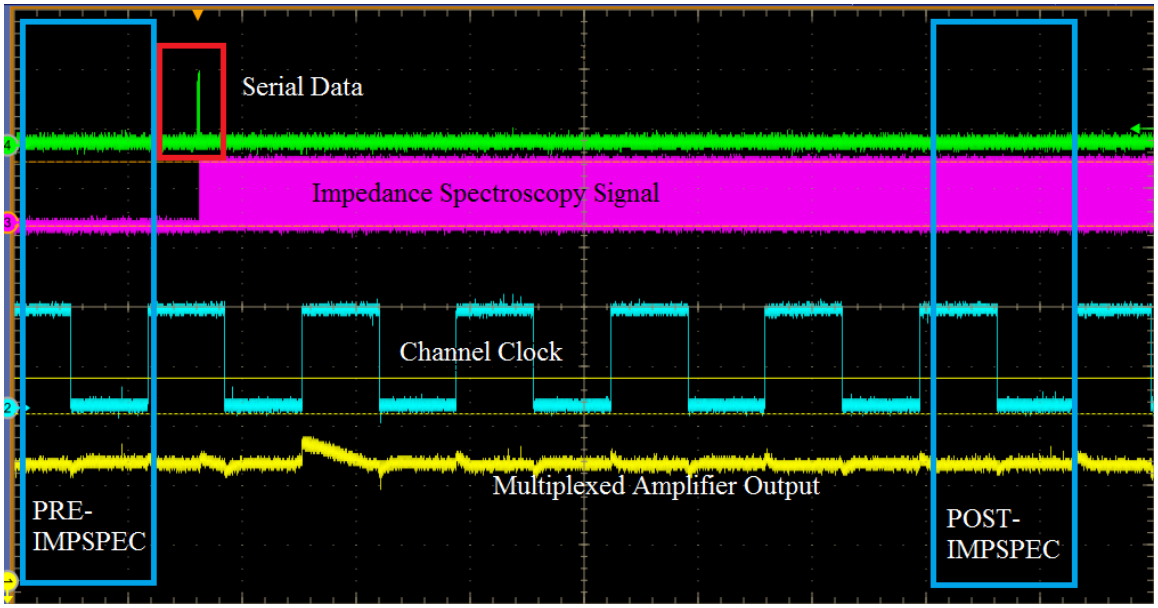


Figure 3.29: Recording performance with and without impedance spectroscopy signal.

i. *Testing of Impedance Spectroscopy Module in its fundamental modes of operation:* This is to establish that each of the design features works as expected. A 100 kΩ resistor connected to the amplifier bond-pad is used to model the external impedance

The first test was to verify operation in nominal impedance mode. A source frequency was selected and the signal was directed to a single amplifier channel. Figure 3. 30 shows the multiplexed amplifier output. After this was verified, the signal was directed to 2 different channels (with sequential data packets indicating the different addresses). The output from this test is shown in Figure 3.31 Next, the signal was then simultaneously directed to all 100 channels as shown in Figure 3.32

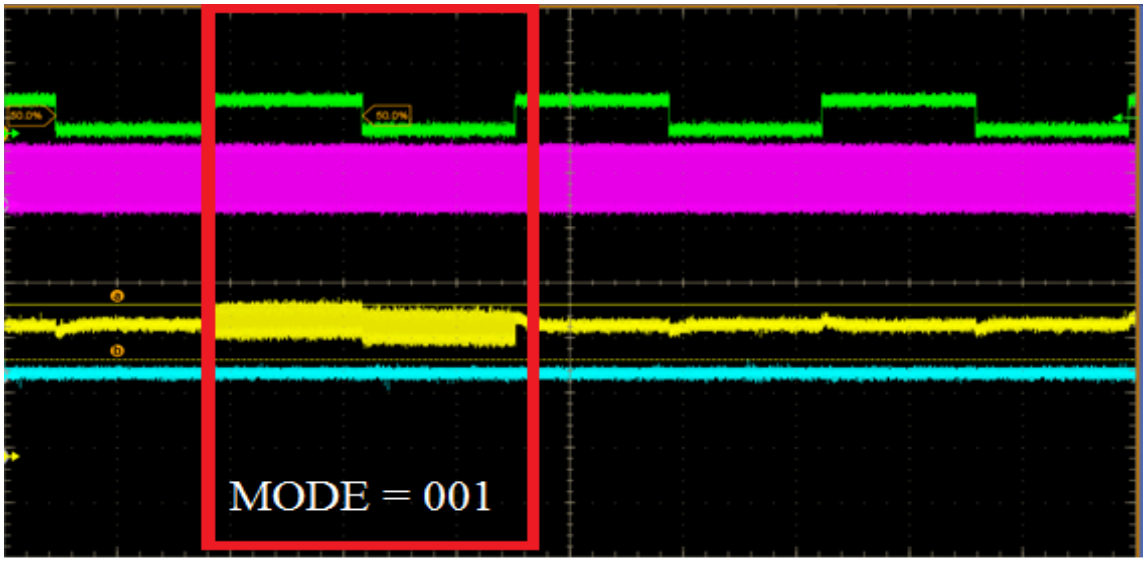


Figure 3.30: Impedance Spectroscopy in nominal impedance mode. The larger output waveform representing the 1mV square wave is evident on the multiplexed output line (yellow) for 1 clock period of the channel multiplexing clock (green). The original impedance signal is shown in pink.

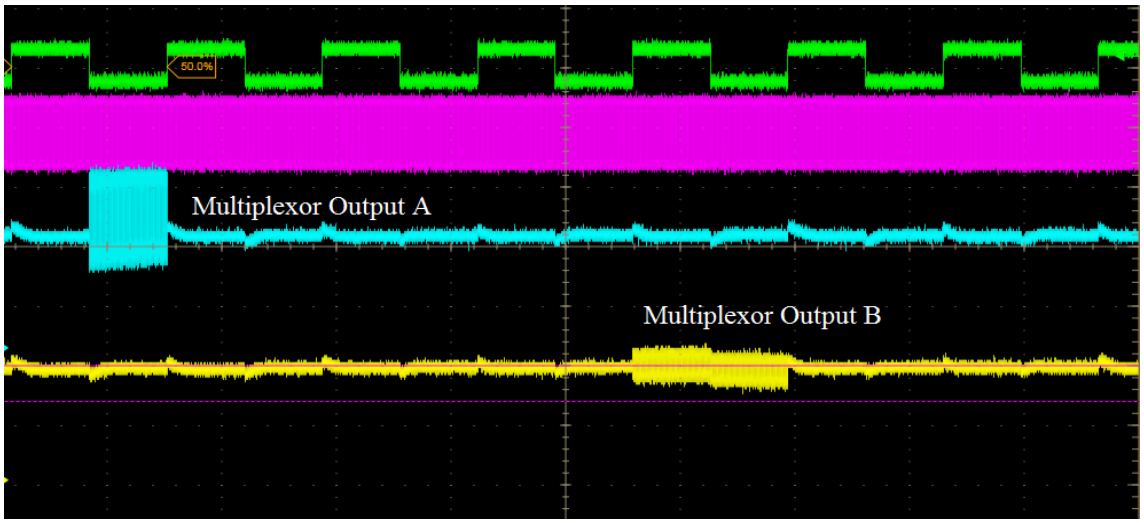


Figure 3.31: Impedance Spectroscopy in nominal impedance mode. Two data packets are sent sequentially. The first one has an address on Bank A and the second with an address on Bank B.

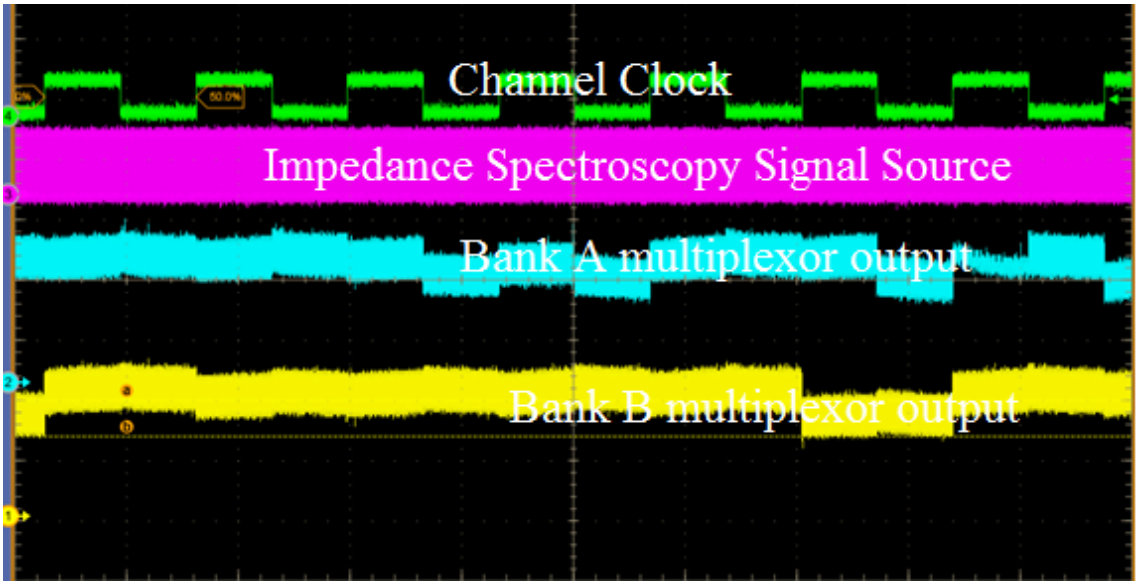


Figure 3.32: Impedance Spectroscopy in nominal impedance mode with signal directed to all channels on both Banks A & B.

These tests verified both the signal generation and the addressing capabilities of the digital controller, and the appropriate function of the analog attenuator. The logic of the signal frequency generation was also verified by looking at the same data on a closer time scale. Figure 3.33 shows one example of a data packet and the corresponding output.

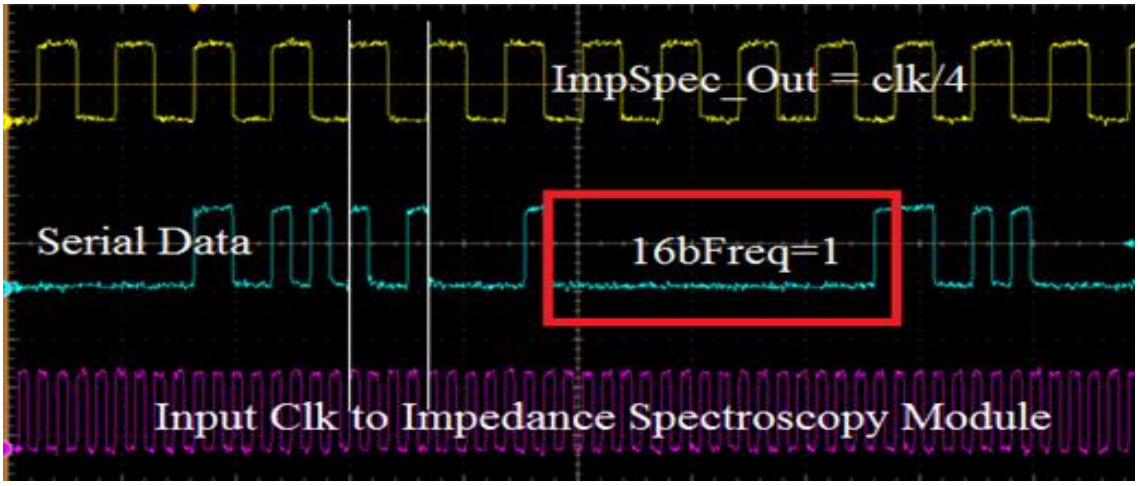


Figure 3.33: Serial data and output of Signal Generation Logic

The final step in bench top verification was to check that the sweep mode was able to generate multiple freuencies according to the design criteria. Figure 3.34 shows two examples of sweep frequencies—the trace on top show a sweep of 2 frequencies while the botton demonstrates a thre frequency sweep.

Figure 3.34: Performance in Sweep mode with 2 (top) and 3 (bottom) frequencies

The ASIC was found to perform as expected in each of the bench top tests as described above. The next step was to incorporate the ASIC into a full recording system platform for further in-vitro and in-vivo testing. The design of a PCB system

and further characterizations obtained from systems level testing are described in Chapter 5.

3.6 References

1. Schwartz AB, Cui XT, Weber Douglas J, Moran DW. Brain-Controlled Interfaces: Movement Restoration with Neural Prosthetics. Neuron. 2006;52(1):205-20.

2. Donoghue JP, Nurmikko A, Black M, Hochberg LR. Assistive technology and robotic control using motor cortex ensemble-based neural interface systems in humans with tetraplegia. The Journal of Physiology. 2007;579(3):603-11.

3. Suner S, Fellows MR, Vargas-Irwin C, Nakata GK, Donoghue JP. Reliability of signals from a chronically implanted, silicon-based electrode array in non-human primate primary motor cortex. Neural Systems and Rehabilitation Engineering, IEEE Transactions on. 2005;13(4):524-41.

4. Nicolelis MAL, Dimitrov D, Carmena JM, Crist R, Lehew G, Kralik JD, et al. Chronic, multisite, multielectrode recordings in macaque monkeys. Proceedings of the National Academy of Sciences. 2003;100(19):11041-6.

5. Rousche PJ, Normann RA. Chronic recording capability of the Utah Intracortical Electrode Array in cat sensory cortex. Journal of Neuroscience Methods. 1998;82(1):1-15.

6. Harrison, Reid R., Paul T. Watkins, Ryan J. Kier, Robert O. Lovejoy, Daniel J. Black, Bradley Greger, and Florian Solzbacher. "A low-power integrated circuit for a wireless 100-electrode neural recording system." Solid-State Circuits, IEEE Journal of 42, no. 1 (2007): 123-133.

7. Eliades, Steven J., and Xiaoqin Wang. "Chronic multi-electrode neural recording in free-roaming monkeys." Journal of neuroscience methods 172, no. 2 (2008): 201-214.

8. Perge, J. A., Homer, M. L., Malik, W. Q., Cash, S., Eskandar, E., Friehs, G., Hochberg, L. R. (2013). Intra-day signal instabilities affect decoding performance in an intracortical neural interface system. Journal of neural engineering, 10(3), 036004

9. Edell DJ, Toi VV, McNeil VM, Clark LD. Factors influencing the biocompatibility of insertable silicon microshafts in cerebral cortex. Biomedical Engineering, IEEE Transactions on. 1992;39(6):635-43.

10. Schwartz AB. Cortical neural prosthetics. Annual review of neuroscience. 2004;27:487-507.

11. Williams, Justin C., Joseph A. Hippensteel, John Dilgen, William Shain, and Daryl R. Kipke. "Complex impedance spectroscopy for monitoring tissue responses to inserted neural implants." Journal of neural engineering 4, no. 4 (2007): 410.

12. Sridharan, A., Rajan, S. D., & Muthuswamy, J. (2013). Long-term changes in the material properties of brain tissue at the implant–tissue interface. Journal of neural engineering, 10(6), 066001.

13. Ward, Matthew P., Pooja Rajdev, Casey Ellison, and Pedro P. Irazoqui. "Toward a comparison of microelectrodes for acute and chronic recordings." Brain research 1282 (2009): 183-200.

14. Grill, W. M., Norman, S. E., & Bellamkonda, R. V. (2009). Implanted neural interfaces: biochallenges and engineered solutions. Annual Review of Biomedical Engineering, 11, 1-24.

15. Indwelling Neural Implants: Strategies for Contending with the In Vivo Environment. 1ed: Taylor & Francis Group, LLC; 2008.

16. Liu, X., McCreery, D. B., Carter, R. R., Bullara, L. A., Yuen, T. G., & Agnew, W. F. (1999). Stability of the interface between neural tissue and chronically implanted intracortical microelectrodes. Rehabilitation Engineering, IEEE Transactions on, 7(3), 15-326.

17. Jackson N, Sridharan A, Anand S, Baker M, Okandan M and Muthuswamy J 2010 Long-term neural recordings using MEMS based movable microelectrodes in the brain. Front Neuroeng. 310

18. Otto, Kevin J., Matthew D. Johnson, and Daryl R. Kipke. "Voltage pulses change neural interface properties and improve unit recordings with chronically implanted microelectrodes." Biomedical Engineering, IEEE Transactions on 53, no. 2 (2006): 333-340.

19. Newbold, C., Richardson, R., Huang, C. Q., Milojevic, D., Cowan, R., & Shepherd, R. (2004). An in vitro model for investigating impedance changes with cell

growth and electrical stimulation: implications for cochlear implants. Journal of neural engineering, 1(4), 218.

20. Moxon, Karen A., Nader M. Kalkhoran, Mathew Markert, Marisa A. Sambito, J. L. McKenzie, and J. Thomas Webster. "Nanostructured surface modification of ceramic-based microelectrodes to enhance biocompatibility for a direct brain-machine interface." Biomedical Engineering, IEEE Transactions on 51, no. 6 (2004): 881-889.

21. He, Wei, George C. McConnell, Thomas M. Schneider, and Ravi V. Bellamkonda. A novel anti-inflammatory surface for neural electrodes. Advanced Materials 19, no. 21 (2007): 3529-3533.

22. Karp, F. B., Bernotski, N. A., Valdes, T. I., Bohringer, K. F., & Ratner, B. D. (2008). Foreign body response investigated with an implanted biosensor by in situ electrical impedance spectroscopy. IEEE Sensors Journal, 8(1-2), 104-112.

23. Dean, D., Ramanathan, T., Machado, D., & Sundararajan, R. (2008). Electrical impedance spectroscopy study of biological tissues. Journal of electrostatics, 66(3),165-177.

24. Duan, Y. Y., Clark, G. M., & Cowan, R. S. (2001). Factors determining and limiting the impedance behavior of implanted bioelectrodes. Paper presented at the Smart Materials and MEMS.

25. Lisdat, F., & Schäfer, D. (2008). The use of electrochemical impedance spectroscopy for biosensing. Analytical and bioanalytical chemistry, 391(5), 1555-1567.

26. Mercanzini, André, et al. "In vivo electrical impedance spectroscopy of tissue reaction to microelectrode arrays." Biomedical Engineering, IEEE Transactions on 56.7 (2009): 1909-1918.

27. Lempka, S. F., Miocinovic, S., Johnson, M. D., Vitek, J. L., & McIntyre, C.C. (2009). In vivo impedance spectroscopy of deep brain stimulation electrodes. Journal of neural engineering, 6(4), 046001.

28. Polikov VS, Tresco PA, Reichert WM. Response of brain tissue to chronically implanted neural electrodes. Journal of Neuroscience Methods. 2005;148(1):1-18.

29. McConnell, G. C., Butera, R. J., & Bellamkonda, R. V. (2009). Bioimpedance modeling to monitor astrocytic response to chronically implanted electrodes. Journal of neural engineering, 6(5), 055005.

30. Joye, Neil, Alexandre Schmid, and Yusuf Leblebici. "Electrical modeling of the cell–electrode interface for recording neural activity from high-density microelectrode arrays." Neurocomputing 73.1 (2009): 250-259.

31. McAdams, E. T., A. Lackermeier, J. A. McLaughlin, D. Macken, and J. Jossinet. "The linear and non-linear electrical properties of the electrode-electrolyte interface." Biosensors and Bioelectronics 10, no. 1 (1995): 67-74.

32. McAdams, E. T., and J. Jossinet. "Tissue impedance: a historical overview." Physiological measurement 16.3A (1995): A1.

33. Dymond, Anthony M. "Characteristics of the metal-tissue interface of stimulation electrodes." Biomedical Engineering, IEEE Transactions on 4 (1976): 274-280.

34. Yu, Tony, Valerie J. Tutwiler, and Kara Spiller. "The Role of Macrophages in the Foreign Body Response to Implanted Biomaterials." In Biomaterials in Regenerative Medicine and the Immune System, pp. 17-34. Springer International Publishing, 2015.

35. George CM, Howard DR, Allan IL, Claire-Anne G, Robert EG, Ravi VB. Implanted neural electrodes cause chronic, local inflammation that is correlated with local neurodegeneration. Journal of Neural Engineering. 2009;6(5):056003.

36. Sawyer, A.J. and Kyriakides, T.R., 2013. Nanoparticle-based evaluation of blood–brain barrier leakage during the foreign body response. Journal of neural engineering, 10(1), p.016013.

37. Biran, Roy, Dave C. Martin, and Patrick A. Tresco. "The brain tissue response to implanted silicon microelectrode arrays is increased when the device is tethered to the skull." Journal of Biomedical Materials Research Part A 82, no. 1 (2007): 169-178.

38. Prasad, Abhishek, Qing-Shan Xue, Robert Dieme, Viswanath Sankar, Roxanne C. Mayrand, Toshikazu Nishida, Wolfgang J. Streit, and Justin C. Sanchez. Abiotic-biotic characterization of Pt/Ir microelectrode arrays in chronic implants.(2014): 1-15.

39. Skousen JL, Bolick K, Bridge M, Tresco PA. A predictive model of the foreign body response to devices implanted chronically in the central nervous system. brain. 2012;1:3.

40. Barsoukov, E., & Macdonald, J. R. (2005). Impedance spectroscopy: Theory,experiment, and applications: Wiley. com.

41. Gunalan, K., Warren, D. J., Perry, J. D., Normann, R. A., & Clark, G. A. (2009). An automated system for measuring tip impedance and among-electrode shunting in high-electrode count microelectrode arrays. Journal of neuroscience methods, 178(2), 263-269.

42. Wang, C., Brunton, E., Haghgooie, S., Cassells, K., Lowery, A., & Rajan, R. (2013). Characteristics of electrode impedance and stimulation efficacy of a chronic cortical implant using novel annulus electrodes in rat motor cortex. Journal of neural engineering, 10(4), 046010.

43. Mancini R. Opamps for everyone: Texas Instruments; August 2002.

44. Lindberg, E., ‘‘Oscillators—An Approach for a Better Understanding,’’ Proceedings of the 2003 European Conference on Circuit Theory and Design, Krakow, Poland, 2003.

45. Sher, Anna A., Alan M. Bond, David J. Gavaghan, Kathryn Gillow, Noel W. Duffy, Si-Xuan Guo, and Jie Zhang. "Fourier Transformed Large Amplitude Square-Wave Voltammetry as an Alternative to Impedance Spectroscopy: Evaluation of

Resistance, Capacitance and Electrode Kinetic Effects via an Heuristic Approach." Electroanalysis 17, no. 15-16 (2005): 1450-1462.

46. Itkis, Michael, Jamshid BG Ghajar, and Robert J. Hariri. "The square-wave approach to impedance measurement of brain tissue water dynamics." Journal of neuroscience methods 59, no. 2 (1995): 237-244.

47. Dyer, C. K., and J. S. L. Leach. "Electrode impedance measurements at short times by a square-wave technique." Electrochimica Acta 19, no. 11 (1974): 695-700.

Chapter 4. Evaluation of Impedance Spectroscopy in Benchtop, In-vitro and In-vivo Tests

The design, simulation and basic benchtop characterizations using a bread-board and packaged Impedance Spectroscopy ASIC are described in Chapter 3. This chapter addresses the systems level testing of the ASIC in more extensive bench top, in-vitro and in- vivo tests.

4.1 A Prototype Test System, Data Acquisition and Command Delivery

The 100-channel Impedance Spectroscopy ASIC was used to build a 32-channel wired prototype test system. The choice of a reduced channel count was made for quick assembly (the 100-channel system requires flip-chip bonding of the ASIC through a contractor while the 32-channel system may be assembled in-house through wire-bonding). Ease of use with rodents (which are the test platform of choice) was another reason for this choice. The PCB-based system was designed to use a 36-channel Omnetics mating connector [1] to connect with a 6x6 Utah MEA.

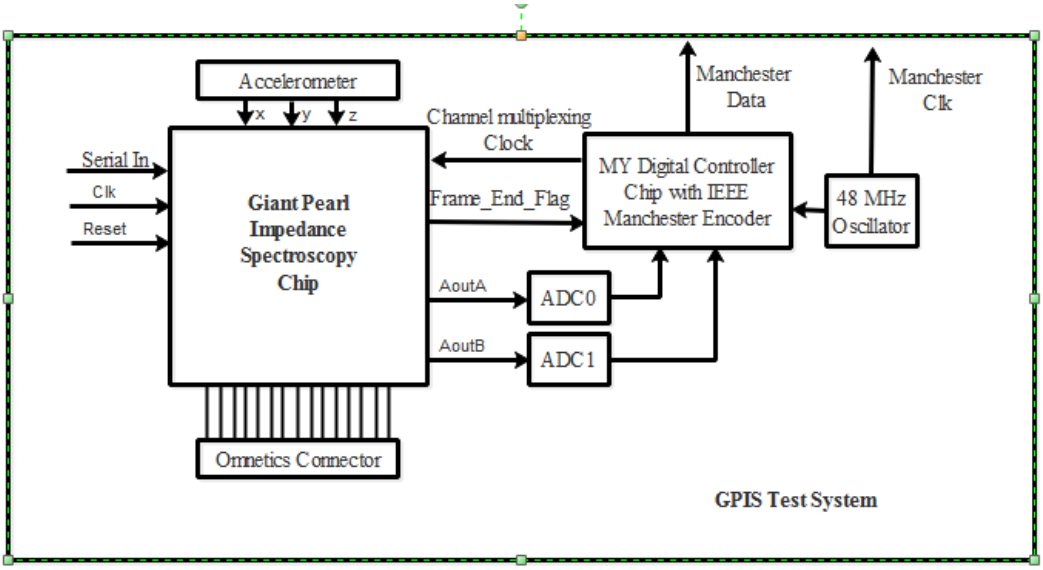


Figure 4.1: Overview Block Diagram of the Impedance Spectroscopy ASIC Evaluation System.

Figure 5.2 shows the PCB layout and the 1x1 inch fabricated board with a rodent-compatible Omnetics connector. The PCB was populated by MultiLab systems in Lawrence, MA (except the amplifier ASIC, which was populated and wire-bonded in-house). A second set of PCBs were populated and tested by a collaborating group, Swiss Center for Electronics and Microtechnology in Neuchatel, Switzerland as part of an ongoing collaboration described in Chapter 6 and Appendix I.

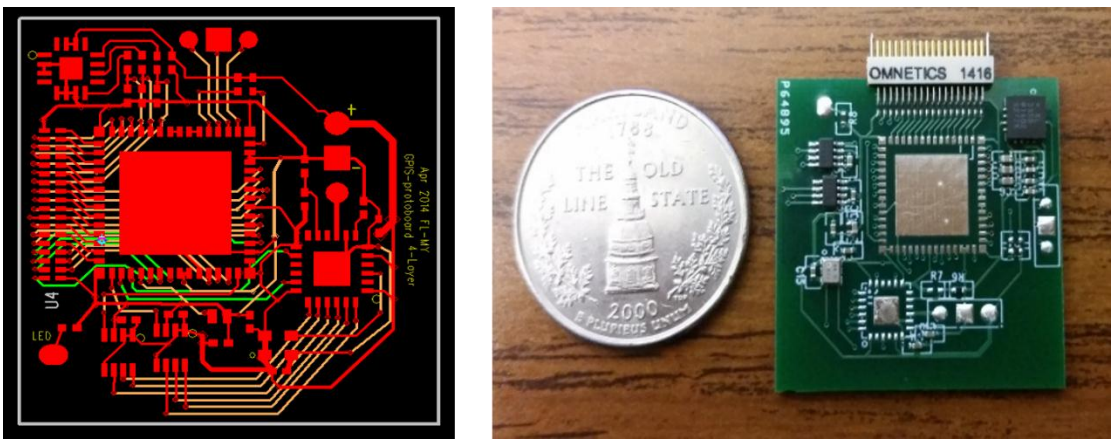


Figure 4.2: 32-channel Impedance Spectroscopy Prototype System PCB layout and fabricated board.

Wired Manchester encoded digital data from the Impedance Spectroscopy proto board is routed to a custom designed Single-In Multiple Out (SIMO) distribution board. An OrangeTree Zest-ET1 Gigabit Ethernet board with a Spartan 3A XCS1400A FPGA [2] is custom programmed to receive data, which involves decoding the Manchester stream and deserializing the data.

Impedance commands to be transmitted to the chip are done using a Xilinx Spartan 3E FPGA. Command delivery and data acquisition will eventually be merged to utilize the same FPGA, but are kept separate at this time due to easy of generating triggers (using the FPGA reset button on the Spartan 3E) without disrupting data capture.

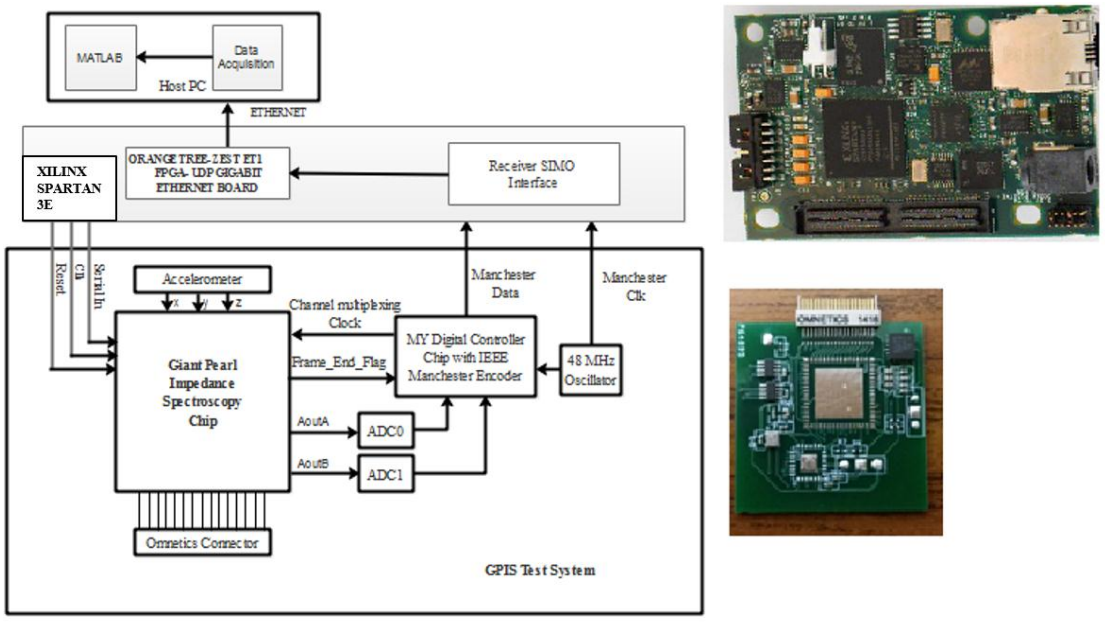


Figure 4.3: (a) (Left) Overview Block Diagram with external components added. (b) (Right Top) OrangeTree Zest ET1 Gigabit Ethernet Board (c) (Right Bottom) Impedance Spectroscopy Test system.

Data is processed using MATLAB. Time domain data presented in the rest of this chapter is raw and unfiltered. Calculation of Impedance values relies on the ratio

of open and closed circuit signal magnitudes. In order to have minimal impact on phase information, data is not filtered or windowed. ADC output values are directly converted into the frequency domain using Discrete Fourier Transform A ratio of the spectral values at the frequency of interest then serves as a proxy for the test impedance (in comparison to an internal calibration resistance).

4.2 Bench-top Calibration Testing with Passive Components

4.2.1 Developing an Accurate Electrical Model of Microelectrode Array for Bench-top Testing

A metal electrode immersed in electrolyte has an impedance given by 4.1:

$$H(j\omega) = R_{electrolyte} + \frac{R_{electrode}}{1+j\omega R_{electrode} C_{double\_layer}} \quad (4.1)$$

In order to obtain a reasonable electrical model of a typical implantable electrode, a commercial impedance testing system (NanoZ™ from White Matter LLC) was used to measure impedances of a 6x6 Utah MEA immersed in 0.9% normal saline. Figure 4.4 shows the impedances of 31 electrodes across a range of frequencies from 1Hz – 2 kHz. This data was then fitted using MATLAB as shown in Figure 4.5, and yielded values for an RC combination to use in bench top characterizations.

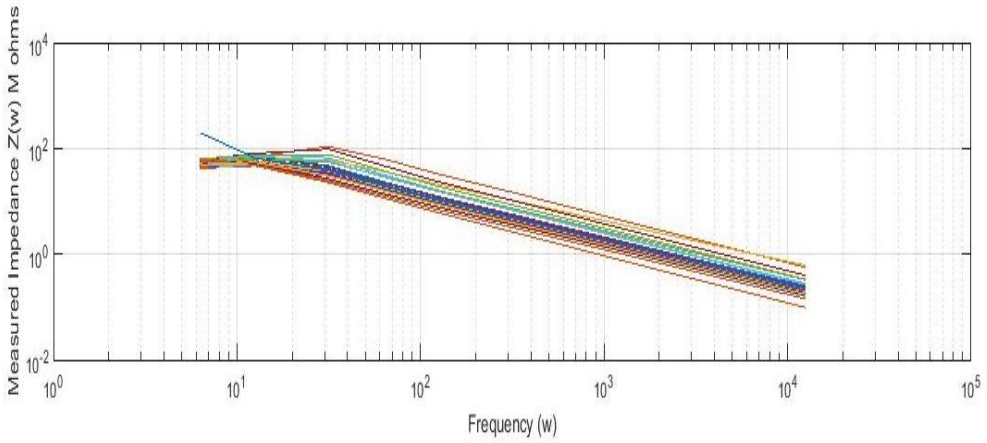


Figure 4.4: Impedance versus frequency measurements from 31 electrodes in a single Utah MEA using NanoZ™

Electrode	Resistance (MΩ)	Capacitance (pF)	16	80.7061	146.07
1	57.9742	678.96	17	67.3783	200.77
2	57.9688	1000	18	65.4843	463.1
3	65.6488	618.65	19	81.1038	340.64
4	66.5307	513.29	20	87.1221	369.64
5	73.2642	554.26	21	100.0984	193.02
6	96.1855	337.24	22	63.855	525.2
7	69.9238	666.08	23	56.8754	640.78
8	69.7511	603.06	24	61.5848	562.86
9	57.9812	693.67	25	62.6712	644.88
10	57.934	492.68	26	101.334	266.71
11	57.1634	527.39	27	64.4468	761.68
12	81.2011	682.33	28	89.1428	840.75
13	86.9144	657.48	29	330.1	803.66
14	73.3387	488.64	30	98.2624	985.75
15	72.3161	462.06	31	63.1795	699.81

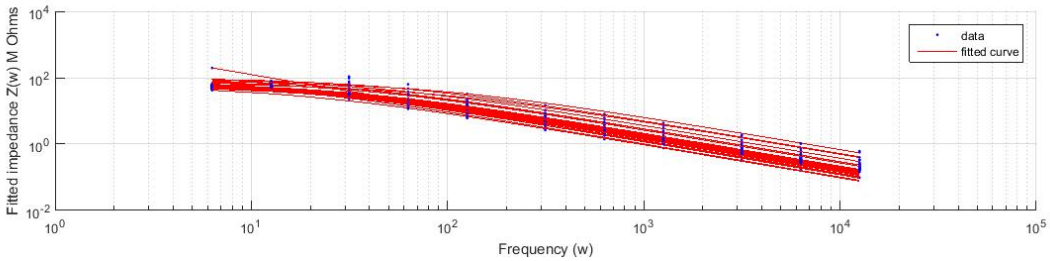


Figure 4.5: Impedance data from Utah MEA, fitted using MATLAB.

The data from the 31 channels was averaged (after removal of outliers) to yield a 55 MΩ resistance in parallel with a 680 pF capacitance as the nominal silicon microelectrode model. Equation 4.1 can thus be rewritten as 4.2 for a Utah MEA electrode.

$$Z(j\omega) = 55\ M\Omega + \frac{1}{(j\omega)\ 680\ pF} \quad (4.2)$$

4.2.2 Bench top calibration testing:

The first functional test was to measure the open circuit voltages in impedance spectroscopy mode across all 100 channels (all channels are simultaneously tied to the impedance source and the output data stream samples across the entire chip, even in the 32-channel system). This is the shown in Figure 4.6 with a 1 kHz source frequency. The amplifiers of channels 21, 41 and 61 in this figure are connected to an on-board accelerometer, and hence do not demonstrate the square wave. Each channel was then grounded to obtain a connector pin to channel number map, demonstrated in Table 4.1.

Omnetics	Amp ch
1	GND
2	71
3	61
4	51
5	-
6	-
7	-
8	13
9	3
10	4
11	5
12	7
13	17
14	8
15	9
16	50
17	60
18	REF

Omnetics	Amp ch
19	REF
20	91
21	82
22	92
23	93
24	94
25	95
26	96
27	97
28	98
29	99
30	89
31	79
32	69
33	20
34	30
35	39
36	GND

Table 4.1: Amplifier channel to Omnetics Pin number map built through use of direct impedance source signal to individual amplifiers.

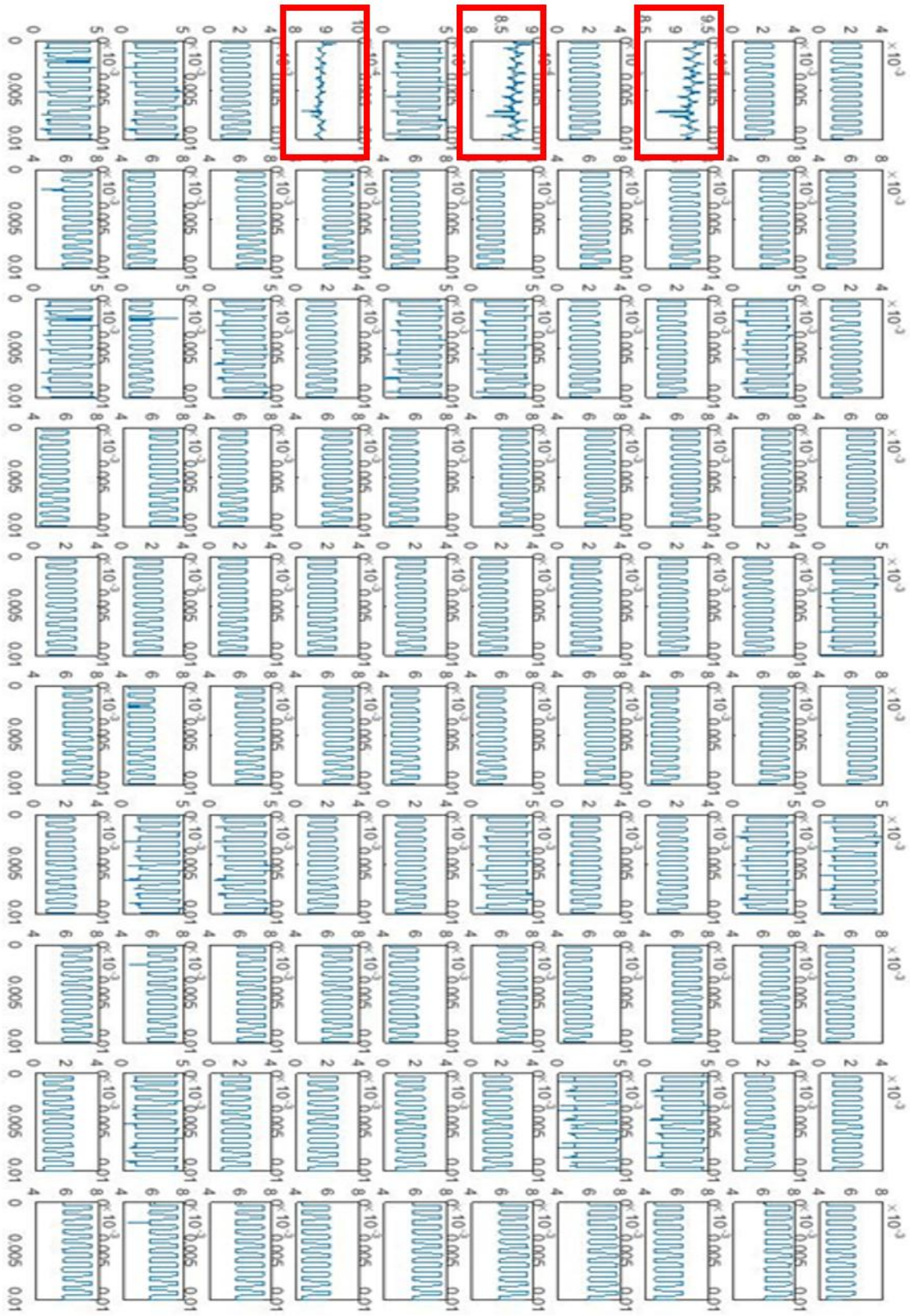


Figure 4.6: Impedance Signal Across 100-channels. Inputs of channels 21, 41 and 61 are connected to an accelerometer, and hence appear "grounded".

Figure 4.7 shows simultaneous grounding of all 32 connected channels. This is used as an calibration test prior to each system use to ensure continued access to all presumed channels.

Figure 4.7: The 32 channel connector is grounded, showing attenuated signals on connected channels only.

4.2.3 Bench top and in-vitro testing

The RC model derived in 4.2.1 was used for measurements described in this section. Impedance source signals of various frequencies were applied to a single electrode loaded with a parallel combination of 55 MΩ and 680 pF, and channel response was measured. Figure 4.8 shows a representative Time and Frequency Domain output pair for a 1 kHz source signal.

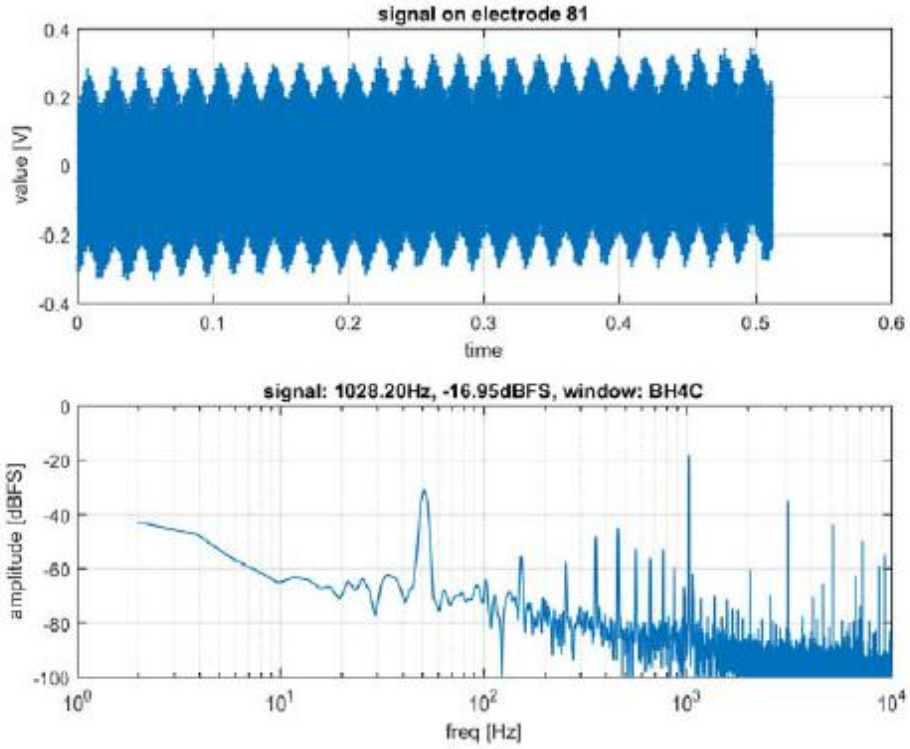


Figure 4.8: (a) (Top) Transient signal with impedance source selected to be 1 kHz. (b) (Bottom) The windowed DFT of the time series in (a) with a signal amplitude of -16.95 dBFS.

Characterization of the ASIC's range and resolution was pursued next. Measurements were done at 1 kHz. RC load impedance was swept from 1kΩ to 5MΩ (by varying capacitance), and recorded ADC output was measured. A linear response is expected as demonstrated in Figure 4.9. At ~750kΩ however, the load capacitance (C = 328pF) forms a low-pass filter with the 500kΩ internal calibration resistor, and an attenuated AC signal can no longer be detected at the output due to this low-pass filter.

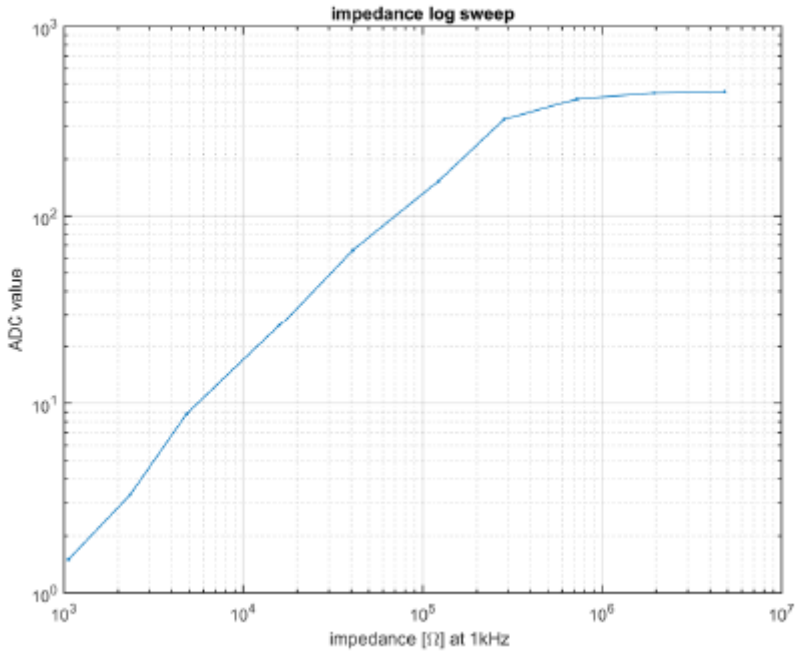


Figure 4.9 : Logarithmic impedance sweep from 1 kΩ to 5MΩ at 1 kHz.

The resolution of the system was characterized next. This is defined as the minimum impedance change that may be reliably detected at the system output, and depends on the signal to noise ratio of the impedance signal to the recording amplifier noise (the latter is described in Chapter 2, and is known from bench top measurements to be ~2.83 μV_{RMS} at 1 kHz). According to these 12-bit ADCs running at 3.3 V, the ADC step correlates with a ΔV of 4 μV at the amplifier input node. An SNR>2 then requires a $\Delta V > 8$ μV (2 ADC steps). At 1 kHz and a nominal 100 kΩ impedance, this yields a resolution of 1 kΩ. This is verified experimentally using a parallel combination of a 55 MΩ resistor and a 1.3 nF capacitor to serve as a base impedance of 104 kΩ. Total impedance is linearly swept in 1kΩ increments between 1kΩ – 18kΩ using a second parallel capacitor. Figure 4.10 shows the recorded ADC output for this linear sweep.

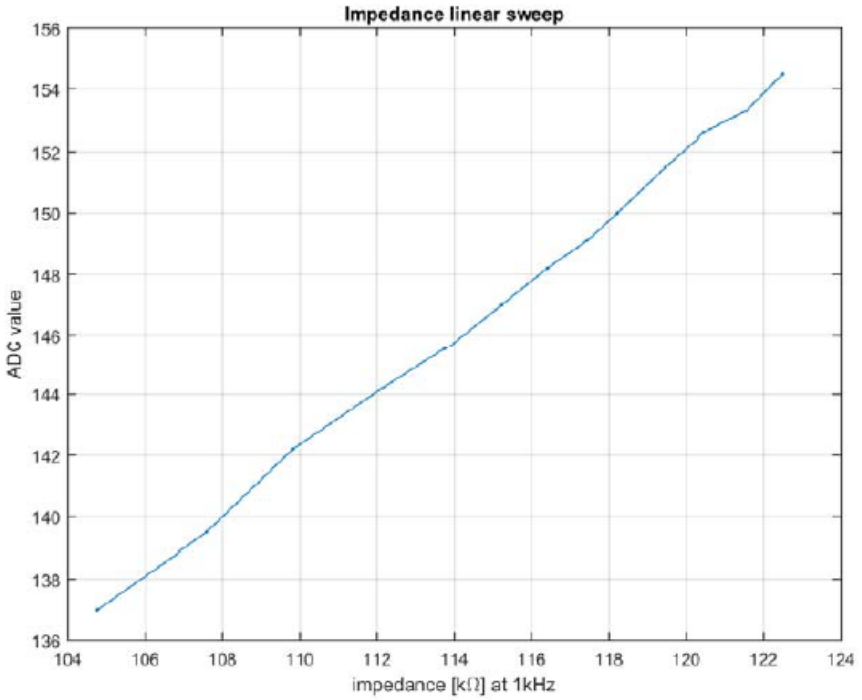


Figure 4.10: Impedance Spectroscopy ASIC Output for a linear impedance sweep from 104 – 122 kΩ at 1 kHz.

The system was then used to characterize the frequency response at a single channel between 40 Hz – 2 kHz. Figure 4.11 summarizes this measurement; the open circuit voltage remains stable across frequencies while the closed system reacts to the increasing capacitive contributions to impedances with increasing frequency. Coupled 60 Hz noise is a significant issue when making bench top measurements with this system, and this is evident in the open circuit response at very low frequencies.

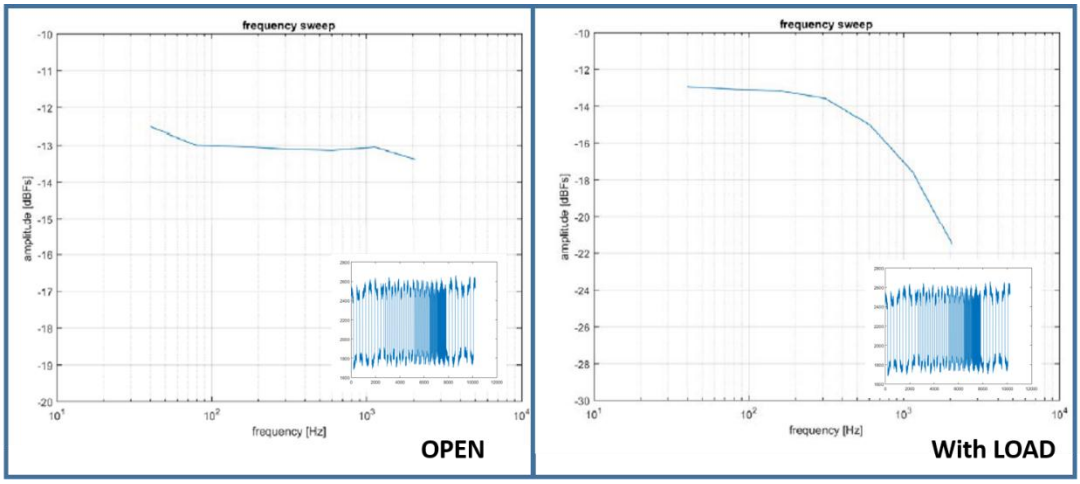


Figure 4.11: Impedance Response to Frequency Sweep from 40 Hz to 2 kHz in open (Left) and closed circuit (Right) configurations.

Finally, the system was tested with a saline-immersed 6x6 Utah MEA. Measurements from the system were compared against vendor-provided values. Figure 4.12 shows the measurement setup. The Utah MEA has 2 Pt-IR reference wires. One is internally grounded through the Impedance Spectroscopy test system while the other is left floating. The measured Time domain impedance response across the 32 connected channels is shown in Figure 4.13. Table 4.2 shows vendor-furnished and measured impedance values.

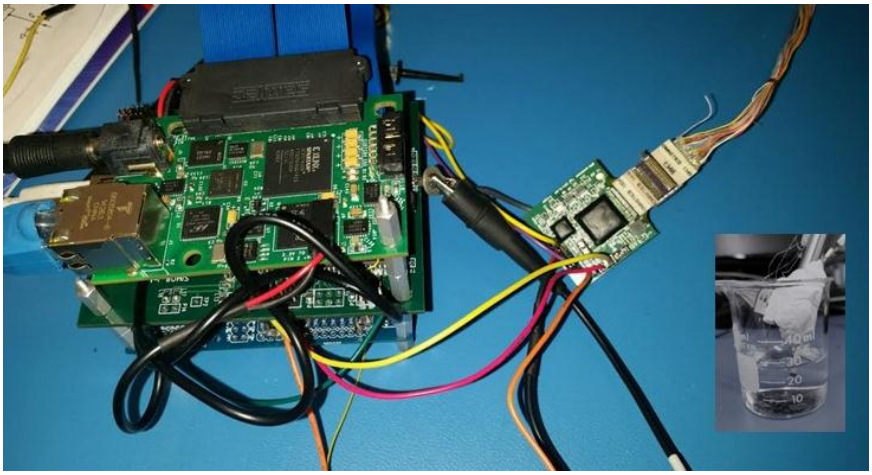


Figure 4.12: Impedance Measurement setup for in-vitro measurements with Utah Array in Saline.

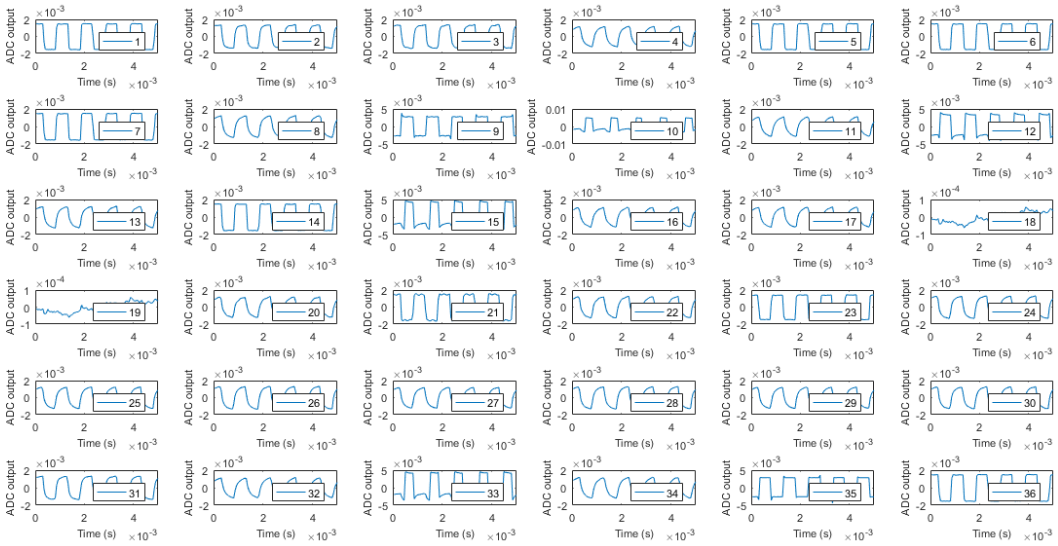


Figure 4.13: Transient response to 1 kHz signal across 32 connected channels.

Omnetics	Vendor Values (kΩ)	Measured Values (kΩ)
1	GND	GND
2	457	167
3	437	223
4	262	155
5	278	NC
6	355	NC
7	514	NC
8	207	167
9	221	1000
10	215	765
11	435	135
12	154	1231
13	154	161
14	160	288
15	202	1000
16	143	136
17	174	142
18	REF	REF

Omnetics	Vandor Values (kΩ)	Measured Values (kΩ)
19	REF	REF
20	234	156
21	195	287
22	270	165
23	202	268
24	220	185
25	202	170
26	340	187
27	185	160
28	212	179
29	186	166
30	247	177
31	237	203
32	186	141
33	185	1000
34	240	152
35	270	1000
36	GND	GND

Table 4.2: Impedance values of 6x6 Utah MEA in saline.

Table 4.2 demonstrates that several impedance values are in the same ballpark as vendor supplied values but are not identical. Some of this error could be associated with resistor sizing variability (we use a standard calibration value for all

computations). This needs to be investigated further and addressed appropriately. The larger deviations from vendor-supplied values are likely either due to post-calibration electrode damage (causing increase in impedance) or previous use debris on electrode (causing decrease in impedance). The latter is likely to happen since this acute array has been used several times for acute animal experiments.

The saline data does nonetheless demonstrate that the attenuated signals can be processed and that the impedance values generated are close in magnitude to the expected numbers. Since vendor-provided values only included a magnitude for impedance, the data processing approach did not focus on extraction of phase information, which is discussed in the next section.

4.3 animal Testing with the Impedance Spectroscopy ASIC

In-vivo testing of the impedance spectroscopy system was conducted in a Long-Evan rat with a 6x6 implanted Utah MEA. The animal has been implanted for >6 months and has had stable recordings during this time.

Figure 4.14: Animal experimental setup with Utah MEA connected to Impedance Spectroscopy Test syste m through a multi-channel cable connector.

Figure 4.15 shows a comparison between the open and closed circuit Time and Frequency domain signals at one channel.

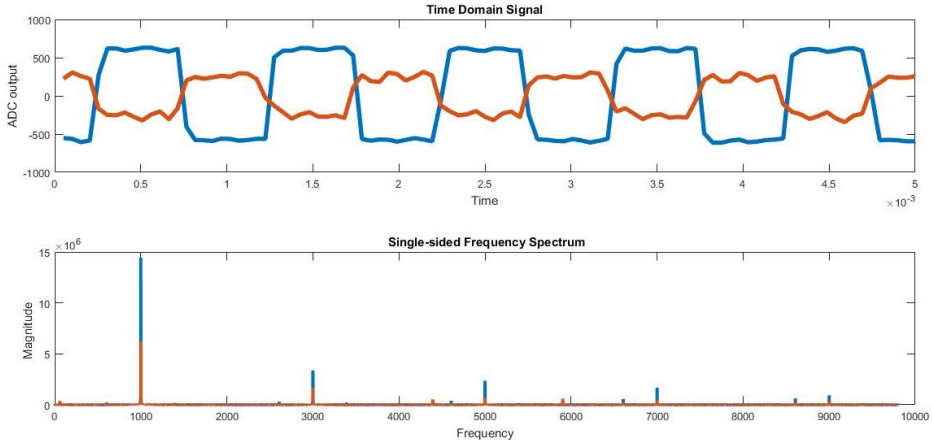


Figure 4.15: Open and Closed Circuit Impedance Signals at one channel in an animal with Utah MEA

In order for these signals to be used effectively for extraction of phase information, they need to be temporally aligned appropriately. The latter highlights a limitation of the current data acquisition system, which is unable to process an external synchronization trigger along with the Manchester-encoded output data

stream. For the purposes of this experiment, the signals were aligned manually by matching the phase of the unconnected open channels. Figure 4.16 demonstrates the transient signals of the 6x6 array. It can be seen that the closed circuit phase of different channels varies in comparison to the open circuit calibration signal, indicating that phase information may be decoded from the signals.

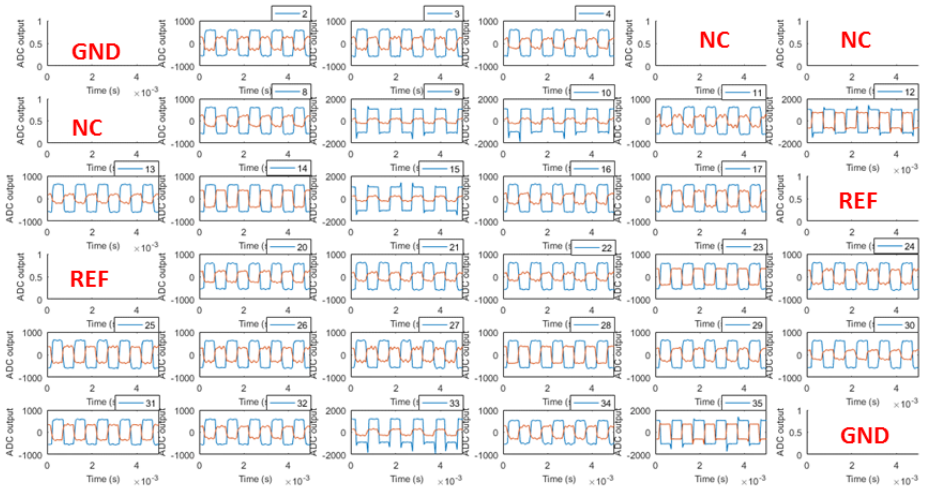


Figure 4.16: Open and Closed Circuit Transient signals from a 6x6 Utah MEA implanted in a rodent.

The impedance values obtained from the test system were then compared with measurements made using a NanoZ™ impedance measurement system for validation. Comparison of these values is shown in Table 4.2. When the measured values are close to expected, they are highlighted in green.

This experiment, along with its in-vitro precursor suggests that the cause of the impedance value mismatch is intrinsic to the test system or data processing software. Only 1 test system was available for use in generating the data presenting in this chapter, and repeating these tests with multiple systems is the first step toward determining the cause of these discrepancies. These experiments have however

validated the basic function of the system and highlighted some issues which are summarized in the next section.

Omnetics	Amp channel	NanoZ (kΩ)	ASIC
1	GND	GND	GND
2	71	262	234
3	61	176	188
4	51	172	146
5	-	OPEN	NC
6	-	416	NC
7	-	488	NC
8	13	441	326
9	3	457	422
10	4	268	234
11	5	OPEN	297
12	7	199	OPEN
13	17	371	217
14	8	356	OPEN
15	9	130	117
16	50	124	144
17	60	128	OPEN
18	REF	REF	REF

Omnetics	Amp channel	NanoZ (kΩ)	ASIC (kΩ)
19	81	REF	REF
20	91	332	374
21	82	286	211
22	92	304	382
23	93	251	OPEN
24	94	599	548
25	95	382	OPEN
26	96	373	538
27	97	333	488
28	98	334	OPEN
29	99	571	419
30	89	261	256
31	79	OPEN	OPEN
32	69	OPEN	443
33	20	OPEN	343
34	30	430	519
35	39	262	OPEN
36	GND	GND	GND

Table 4.2: Impedance Measurements in implanted Utah MEA. NanoZ values compared with measure values from Impedance Spectroscopy Test system.

4.3.1 Current System Limitations and Next Steps

The range of operation for the amplifiers capturing impedance data is +/- 2 mV. The impedance source signal is +/- 3 mV this was chosen to have +/- 0.5 mV at the amplifier input with a nominal 100 kΩ impedance). Full-scale open circuit voltages are thus at clipped by the amplifier rail, and cannot be used in complex impedance calculations. This is, however, a problem that can be easily fixed by adding a board-level resistive divider to tune this full-scale voltage to be within the measurable range.

Another challenge for phase information processing is alignment of signals (as discussed above). This can also be addressed by changing the data acquisition system to incorporate a trigger. An updated board design has already allowed for these changes; these assembled systems will be tested next, both to replicate this data and identify the cause of the noted discrepancies as well as to enable processing of phase information.

Once these tests have been completed, we may consider incorporating a short-range solution for wireless command delivery range IEEE 802.15.4 (Zigbee protocol). Data out can be made wireless by using already designed RF ASIC for a fully wireless system once reliable functionality has been demonstrated.

4.4 References

1. Omnetics 36 channel Nano-Strip connector datasheet. Accessed March 31st, 2016. http://www.omnetics.com/neuro/nano-strip/

2. OrangeTree ZestET1 Gigabit Ethernet Board datasheet. Accessed April 24th, 2016. http://www.orangetreetech.com/zestet1.php.

3. NanoZ Impedance Tester Specs. http://www.white-matter.com/nanoz/. Accessed Mar 30th ,2016.

Chapter 5: "Writing" back to the Brain using Stimulation

5.1 Introduction

Electrical stimulation of the nervous system has a long, rich history and has enjoyed widespread therapeutic use in medicine. Non-focal and non-specific targeting of tissue has been a persistent challenge for this technique, and this has only recently begun to be mitigated by the development of focal probes and IC-based stimulators. Two devices that have been particularly instructive in understanding the principles of CNS stimulation are the Epiretinal and Cochlear Implants, which are shown in Figures 5.1 and 5.2 respectively. Both technologies rely on their respective anatomic (retinotopic/tonotopic) sensory mapping, and effectively demonstrate that even simple sensory commands may be rendered functionally significant through use of patterned stimulation.

The lessons learned from these devices set precedent for patterned intracortical microstimulation as part of a closed-loop neuroprosthesis. Providing meaningful input to the sensorimotor system is not a trivial task, complicated both by the density of sensorimotor representation in cortex as well as the multifocal distribution of neural processing pathways. The latter, however, also offers the possibility to intercept motor pathways at higher level of integration, which is utilized by technologies such as Deep

Brain Stimulators (DBS), Vagus Nerve Stimulators (VNS) and the Neuropace™ Responsive Stimulation System (RNS) as shown in Figure 5.3.

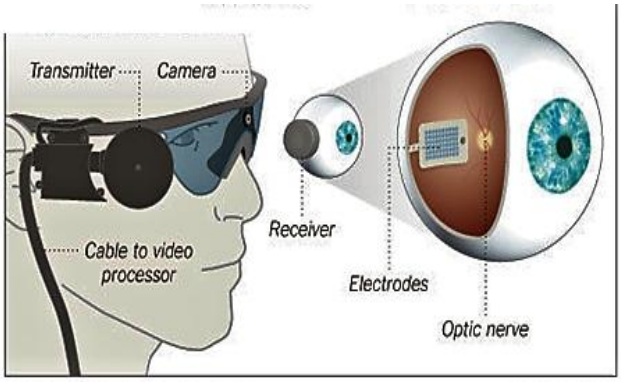


Figure 5.1: The Argus II ® Epiretinal Implant. Targeted for patients with damage and/or loss of retinal photoreceptors as with Retinitis Pigmentosa (RP). The device uses patterned stimulation of retinal ganglion cells driven by images captured by a camera on the eye glasses, processed by a wearable embedded-system computer (termed the Visual Processing Unit (VPU) and transmitted wirelessly to the epiretinal electrode array. Patients are able to perceive spots of light called "phosphenes" and learn to interpret them to use as a visual navigational aid.

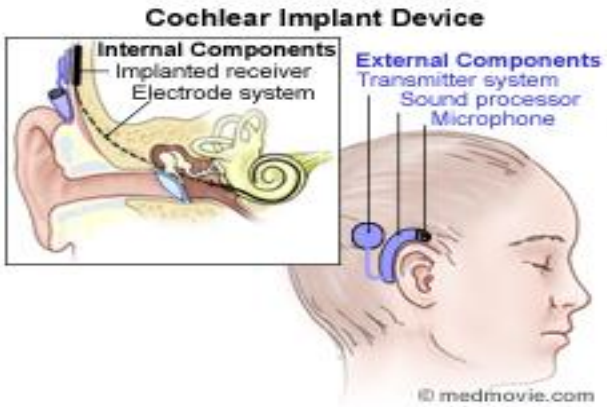


Figure 5.2: Cochlear Implant. Developed for congenital profound sensorineural hearing loss but now also used for acquired age-related sensorineural deafness. Similar to the epiretinal implant with implanted electrodes and wireless telemetry to an external microphone and speech processor.

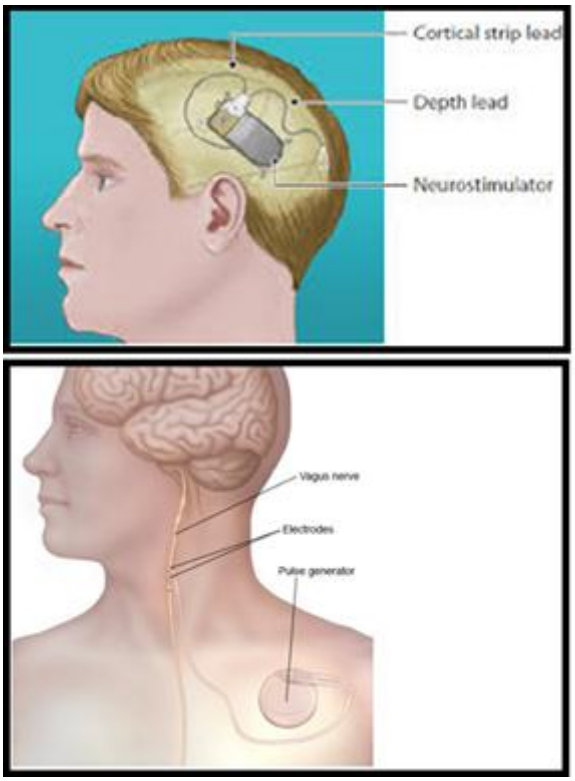


Figure 5.3: (a) (Top) The Neuropace RNS™ system. The system uses a combination of subdural strip and Depth electrodes for sensing and responsive deep brain stimulation (b) (Bottom) Vagus Nerve Stimulator (VNS). A cuff of electrodes is placed around the Vagus nerve in the neck. Continuous low frequency stimulation theoretically inhibits seizures through modulation of brainstem nuclei.

Studies of the therapeutic utility of Intracortical microstimulation (high-frequency continuous and patterned multi-channel) for numerous neurological conditions from epilepsy to stroke and dementia have recently been reported in literature [3-4], indicating that this is a burgeoning opportunity for neuroengineers. Understanding stimulation biophysics is the first step in this direction, and is reviewed briefly below.

5.1.1 Stimulation Electrochemistry and Approaches

The Action Potential (AP), characterized by a stereotypical ~100mV voltage change over ~1ms (shown in Figure 5.4), is the fundamental currency of neural communication [5-6]. It is the result of a vast degree of intra-neural dendritic integration up to the neuron's "depolarization threshold". This threshold is also important from the perspective of stimulator design; the corresponding term is "stimulation threshold" and defines the parameters of efficient coupling between an external electrical stimulus and the effector neuron.

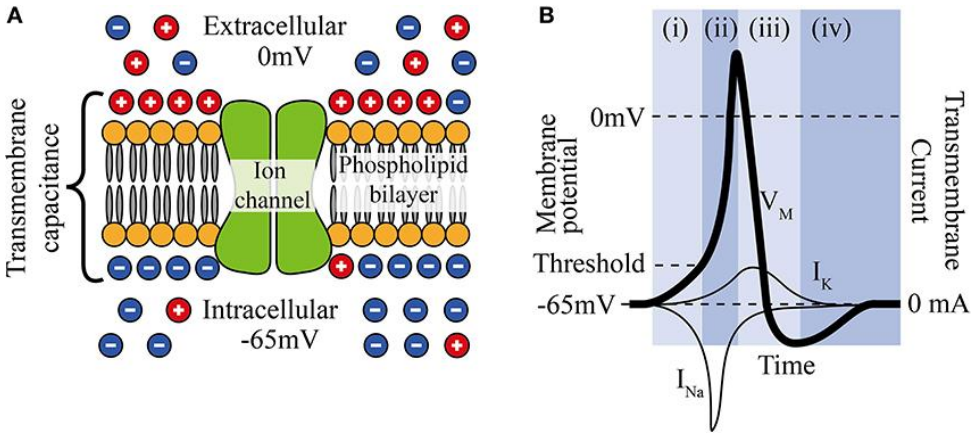


Figure 5.4: The Neural Cell membrane is a functional capacitor with a resting potential across it. This is maintained by the passive diffusion and active transport of ion species across the membrane by ion channels. The membrane may depolarize due to a variety of spatially and temporally summated stimuli; once the collective depolarization crosses the "threshold voltage", it sets into motion the generation of an action potential

Successful electrical stimulation relies on charge transfer across the metallo-ionic electrode-tissue interface described in Chapter 4, as highlighted in Figure 5.5. This may occur through one of two mechanisms: non-Faradaic or Faradaic, where the former relies on charge redistribution while the latter involves actual charge transfer

utilizing redox chemistry at the interface [8-11]. The respective electrochemical changes are reflected in Figure 5.6.

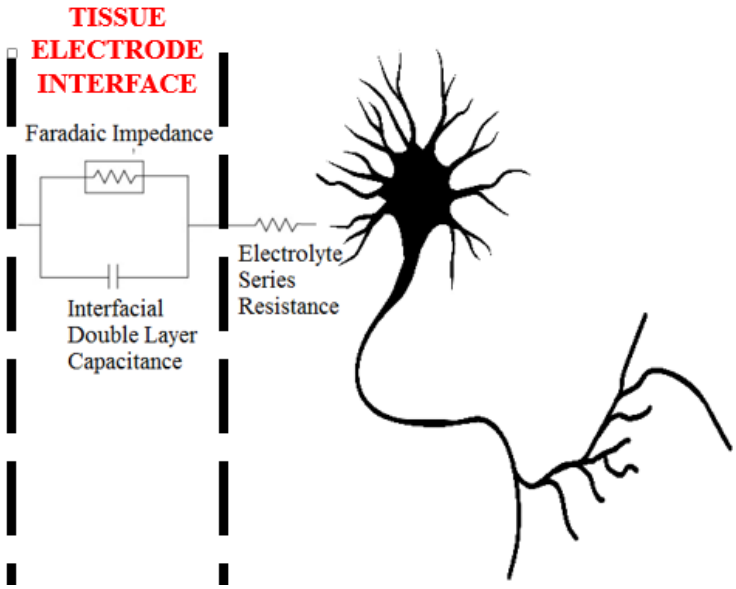


Figure 5.5: A circuit model of the tissue-electrode Interface and its relationship to the excitable Neural Elements. During stimulation, charge is injected into (or removed from) the metal electrode, and couples to tissue through the Faradaic Impedance.

Faradaic processes degrade the interface, and should be minimized in biological stimulation. Faradaic current density is proportional to the interface potential, and electrode materials have to be chosen carefully to minimize contributions from Faradaic processes. Water can also undergo Faradaic oxidation/reduction as demonstrated by 5.1 and 5.2. The interfacial potentials that cause these reactions are termed the "water window" and set the ultimate limits on acceptable interface potentials for biological stimulation.

$$2H_2O + 2e^- \rightarrow H_2 \uparrow + 2OH^- \text{ (reduction of water)} \quad (5.1)$$

$$2H_2O + 2e^- \rightarrow O_2 \uparrow + 4H^+ + 4e^- \text{ (oxidation of water)} \quad (5.2)$$

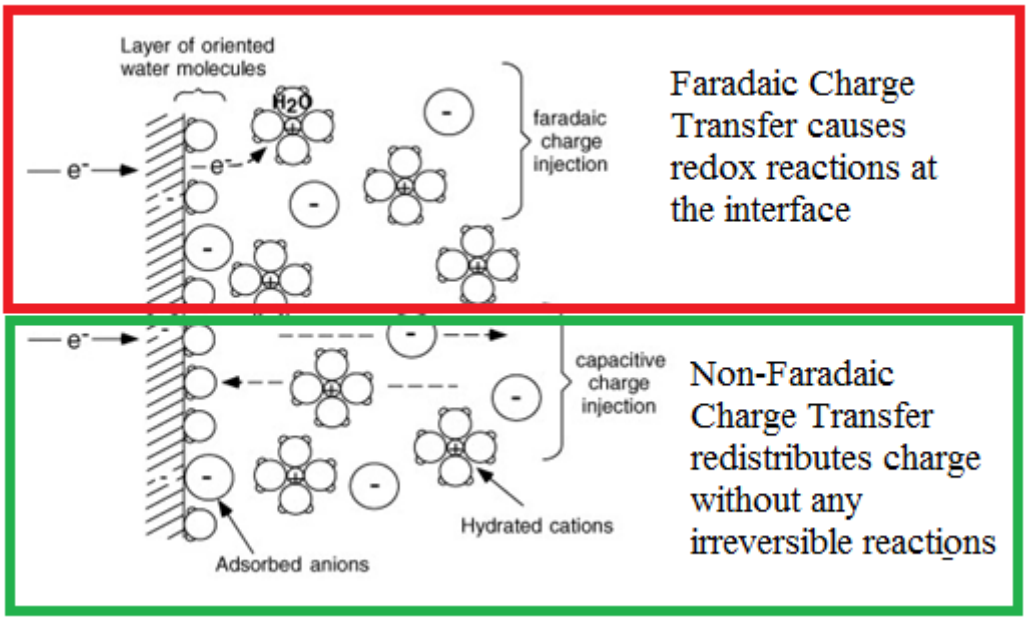


Figure 5.6: Faradaic versus non-Faradaic charge transfer. Faradaic mechanisms causing redox reactions causing the creation of new chemical species. Non-Faradaic mechanisms utilize capacitive coupling and movement of charge carrier species already present in the system.

The charge transfer described above may be accomplished in one of two ways: applying a constant voltage or a constant current. The temporal dynamics of these charge delivery mechanisms is demonstrated in Figure 5.7. Constant voltage stimulation is easy to implement and used in technologies such as DBS. Current magnitude, however, decreases exponentially with time. Moreover, there is no control over its temporal dynamics making it less desirable for high-resolution patterned microstimulation [8, 9, 11]. Hybrid schemes using switched capacitors with constant-voltage stimulation for improved pulse-shaping have been reported in literature [8, 12, 13], but this research is still in early stages, and constant-current stimulation remains the remains the technique of choice for Intracortical microstimulation.

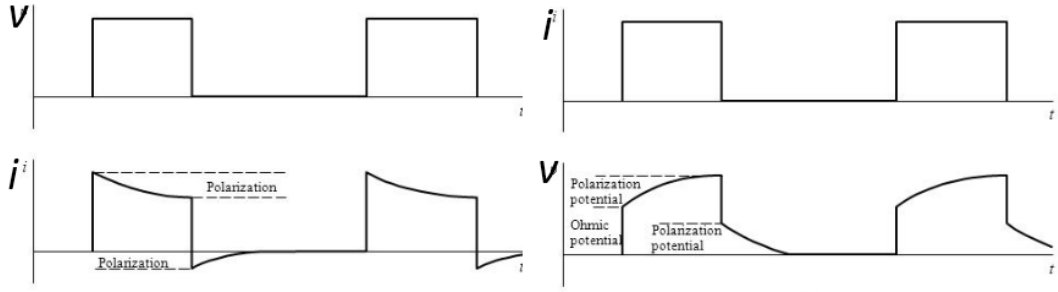


Figure 5.7: Constant Voltage Versus Constant Current Stimulation. (a) (Left) In Constant Voltage Stimulation, current flow decreases exponentially with (b) (Right) In Constant Current Stimulation (right), current amplitude is maintained and the voltage across the interface increases as it "charges up"

5.1.3 Design Considerations for a Patterned Microstimulation

Current Source

The goal of a microstimulation source is to deliver adequate charge for a neuron to cross the stimulation threshold. This must be accomplished within a time frame compatible with patterned stimuli and occur within the "water window". Finally, there should be zero net charge delivery to tissue in order to prevent long-term damage.

Stimulation electrode shape plays an important role in determining the current source specifications through its impact on delivered charge density, which in turn determines both current source focality and current magnitudes for crossing the stimulation threshold. Table 5.1 provides a useful reference to the electrical characteristics of various types of implantable stimulation electrodes. Two key observations from table are that electrodes with higher charge densities are able to cross the stimulation threshold quicker and with lower charge per phase. Secondly, the above mentioned tasks are more readily accomplished by penetrating electrodes.

Their curved geometry is also responsible for their focality (with stimulus radii in 100-200 μm range for a Utah MEA type microelectrode [5]).

Application	Placement	Species	Type	Threshold charge/phase (nC ph^{-1})	Threshold charge density (μC cm^{-2})	Pulse Width (μs)	Reference
Vision	Epi-retinal	Human	Surface	6–1120	5–570	1000	32
Vision	Epi-retinal	Human	Surface	24–100	80–306	2000	33
Vision	Optic nerve	Human	Surface	7–124	4–62	25–400	34
Vision	Intracortical	Human	Penetrating	0.4–4.6	190–2300	200	35
Vision	Cortical	Human	Surface	200,000	11	200	35
Hearing	VCN	Cat	Penetrating	0.75–1.5	60–90	40–150	36, 37
Hearing	AB	Human	Surface[a]	10–200	2.6–52	300	5, 38
Micturition	Intraspinal	Cat	Penetrating	9	4000	100	39
DBS	STN	Human	Penetrating[b]	135–400	2.3–6.7	60–200	40
Motor	Intrafascicular	Cat	Penetrating	4[c]	0.5	50	41
Motor	Sciatic nerve	Cat	Penetrating	5[c]	96	200	42
Motor	Sciatic nerve	Cat	Surface	46	0.35	200	42

Table 5.1: A survey of currently available implantable stimulatory Neural Prostheses [10].

There are two important biological considerations for selecting a stimulation source architecture. Firstly, the large degree of non-linearity in biological systems warrants a stimulator with a large dynamic range to ensure crossing the highly variable stimulation threshold (numbers reported in literature range from a few μA up to a few mA! [5,14-16]). Secondly, the need for a robust mechanism for charge balance warrants the a biphasic, cathode leading stimulus pulse architecture with a well-defined charge recovery period (as demonstrated in Figure 5.8) [14]. The ideal biological stimulator allows control over each of the aspect of the biphasic stimulation pulse highlighted in Figure 5.8 [15-18]. While charge-imbalanced and triphasic stimulation pulses have been reported in literature [18,19] and a stimulator that supports these pulse architectures as well would be desirable, cathode-leading biphasic pulses are the predominant mode of charge delivery in biological systems and thus part of the bare minimum stimulator requirements.

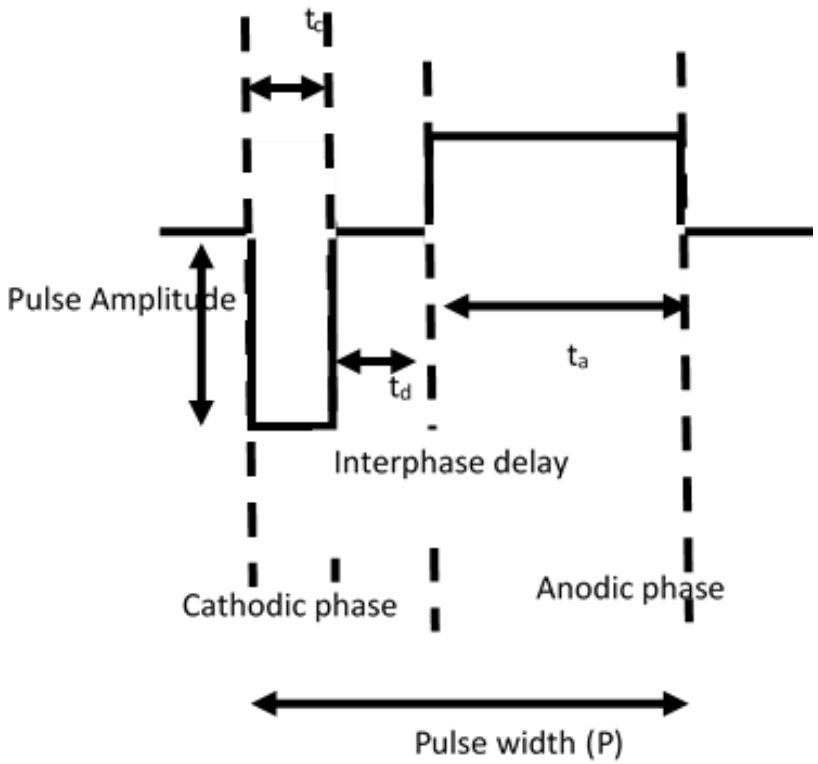


Figure 5.8: The anatomy of a Biphasic Stimulation Pulse. The cathodic phase delivers charge and the anodic phase (which may have a longer phase-width) recovers charge. The inter-phase delay is an important parameter which defines the duration of time the charge imbalance is allowed to persist in the brain.

Current source matching is an important consideration for charge balance. Since well-matched current sources require large silicon area, stimulator architectures typically need to involve a single well-matched source multiplexed between multiple channels. For memoryless stimulators, this sets a latency between patterned stimuli, which is given by 5.3:

$$T_{pulse=}T_{parameter\_load} + T_{charge\ delivery} \tag{5.3}$$

This latency also sets the maximum number of channels that can be multiplexed to a single stimulation source, and can be calculated to be on the order of ~ 100 channels at a stimulation frequency of 20 Hz.

Finally, in the context of closed-loop BCIs, the stimulator design must be compatible with the recording modality. The most significant consideration here is the stimulus artifact, which can saturate recording amplifiers. Hardware and software approaches for artifact cancellation are an active area of research [20-23], but the integrated microstimulator must at minimum be able to decouple the electrodes from the recording amplifier for the duration of stimulation.

5.2 An Integrated Circuit Approach for Simultaneous Intracortical Neural Recording and Microstimulation.

This section describes the IC design for a closed loop recording-patterned microstimulation system constituting a single stimulation engine (composed of a current source and sink for biphasic pulses). The stimulator is integrated with a 16-channel recording amplifier array, as shown in Figure 5.9 The stimulator is designed to be capacitive coupled to the electrode array in order to accomplish charge balance. Furthermore, the switching circuitry at this interface grounds the amplifier at the stimulation site per the requirements outlined in the previous section.

The stimulation engine is implemented as an 8-bit current steering DAC (separate source and sink DACs are designed for biphasic pulse generation). The dynamic range for current amplitude is 20 μA – 3.3 mA.

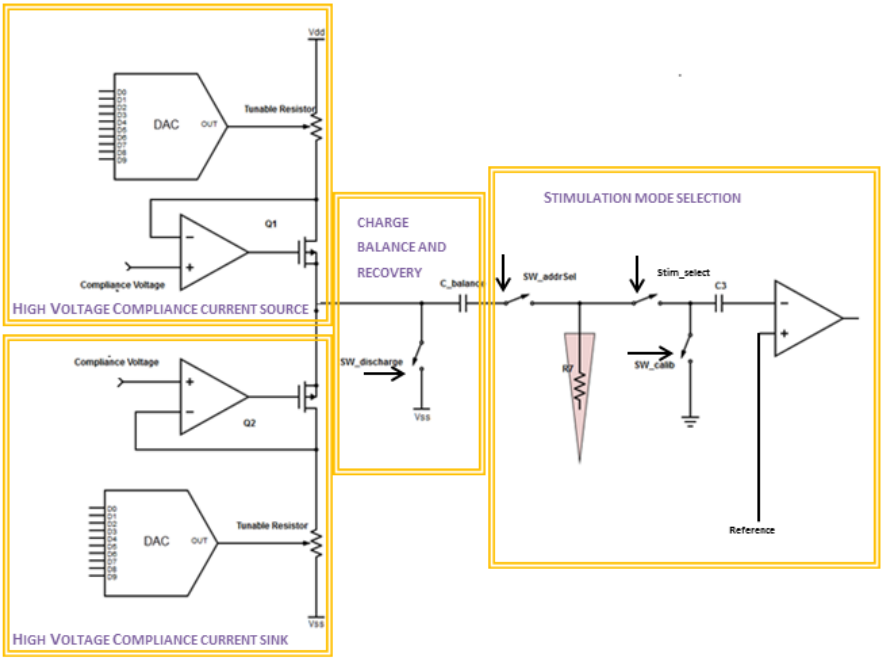


Figure 5.9: Simultaneous multichannel Neural Recording and Stimulation ASIC configuration

A Voltage-controlled resistor (VCR) current-source topology, first described in [26] is implemented. .The number of phases per pulse, pulse frequency and number of pulses (for a pulse train) are user-programmable. Pulse width is set to be a multiple of system clock (with the latter number being user-programmable). Integration with a recording amplifier array is facilitiated through low-resistance (~50Ω) switches.

5.2.1 Bandgap Reference

A dedicated band-gap reference is designed to provide a temperature-independent bias voltage source for the stimulator. Design of a band-gap reference relies on using the negative temperature coefficient of a PN junction in combination with the positive temperature coefficient of thermal voltage V_t to yield a temperature stable reference as shown in Figure 5.10. In CMOS processes, vertical PNP bipolar

transistors are used to create the Proportional-to-Absolute-Temperature (PTAT) element.

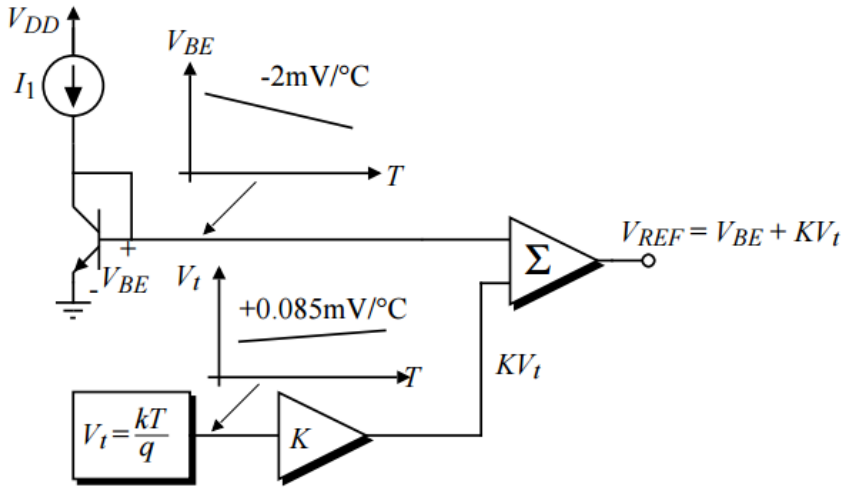


Figure 5.10: A bandgap Reference. The PN junction voltage is Complementary to Absolute Temperature (CTAT) while Thermal Voltage is Proportional to Absolute Temperature (PTAT).

The bandgap reference uses cascoded current sources, and also generates the bias voltages used in the reference current source. Figure 5.11 shows the schematic of the bandgap reference and Figure 5.12 shows the results of transient analysis. V_{ref} is designed to be ~ 2x V_{BE} for this design, and is found to be 1.15V in simulations with a 3.1V supply. The compliance voltages for the source and sink DACs, designed to be 100 mV from supply rails, are found to be 3.02V and 96.73 mV in simulation.

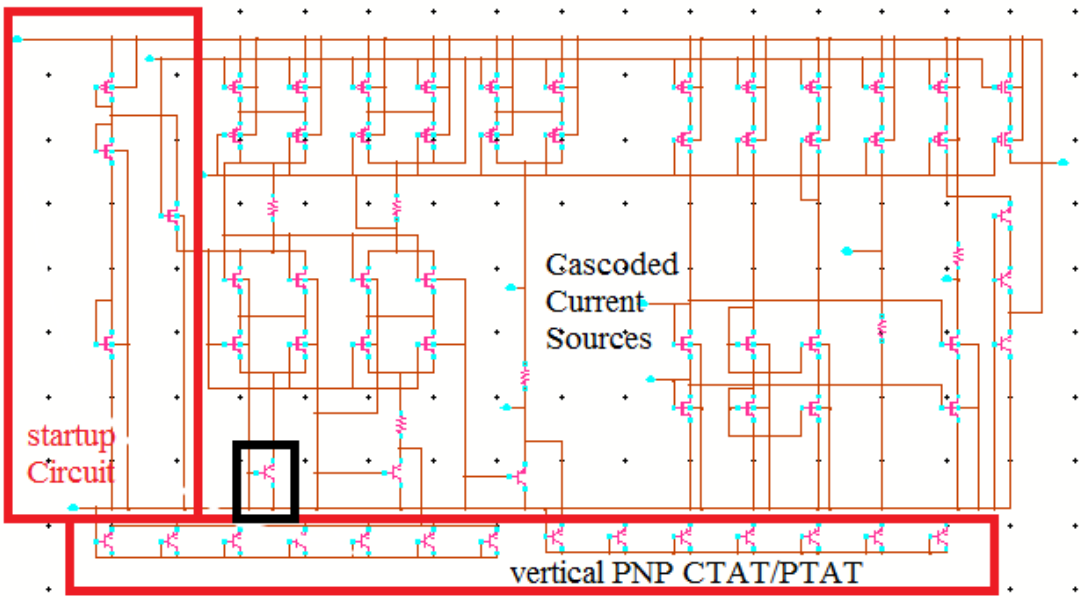


Figure 5.11: Schematic of a Bandgap voltage reference

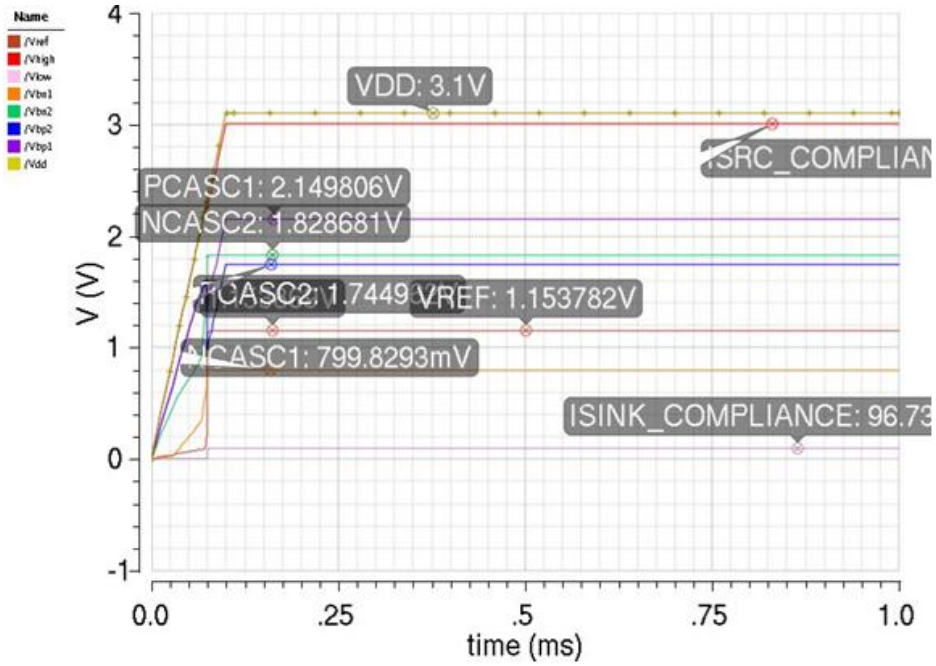


Figure 5.12: Transient analysis of startup and DC stead state Bandgap voltage outputs

5.2.2 DAC programming module

The user-programmable features of the stimulator include pulse parameters as well as stimulus address. These are extracted from a 64-bit serial data packet (described in Table 5.2) by an on-chip logic module. The latter was designed in

VHDL and synthesized using Mentor Graphics Leonardo Spectrum. Power lines for the logic block are isolated from the rest of the chip to conserve power when stimulation is not being used. An 8-bit synch sequence is used to flag the beginning and end of each packet; this provides added security when commands are delivered wirelessly. The DAC programmer does not have any on-chip memory for predefined stimulation parameters. Commands must be provided each time, and there is a 64-bit delay from the start of command to generation of stimulation current.

8 bit SYNCH	Predefined bit sequence determines start of a data packet
3 bit MODE	This indicates whether the system remain in recording mode or switches to stimulator mode.
8 bit address	This is decoded to provide multiplexing of the stimulator output to 1 of 16 channels in this design (but scalable up to 128 channels)
10 bit Stim+	This provides the Digital input to the Current Source DAC
10 bit Stim-	This provides the Digital input to the Current Sink DAC
12 bit Frequency	This provides stimulation frequency (time between pulses). Individual pulse widths are set by incoming clock frequency and not modulated.
5 bit Pulse Count	This allows for programming up to 16 biphasic pulses to be delivered as a burst to a single electrodes site
8 bit SYNCH	This signifies the end of the data packet

Table 5.2: Serial Data packet to DAC programming module

The function of the DAC programmer was tested in simulation; Figure 5.13 shows delivery of a data packet requesting bipolar stimulation, and the ensuing source and sink DAC enable signals at the end of data packet receipt.

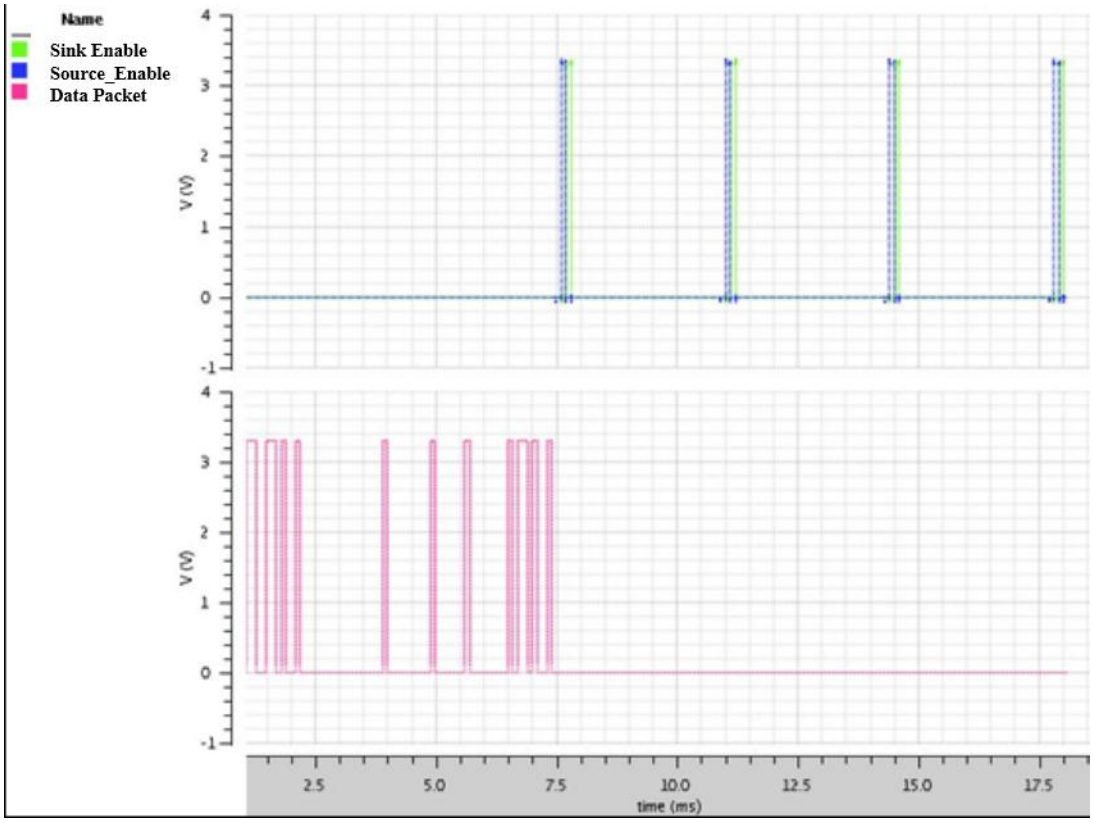


Figure 5.13: A single data packet instructing biphasic stimulation pulses. Source and sink DAC enable signals are generated at the end of data packet delivery.

5.2.3 Source and Sink DAC Design

The Current-steering DAC design relies on a voltage-to-current conversion circuit. Typical implementations of current DACs employ scaled current mirrors. These devices in these standard mirrors have to remain in saturation for operation and the V_{DS} voltage drop across the device reduces its voltage compliance limit. A high compliance voltage is desirable in implantable stimulation sources in order to optimize the supply voltage versus stimulation current ratio. In this implementation, we use a MOS transistor biased in deep-triode region (defined as $V_{GS} - V_{TH} > 2\ V_{DS}$). This functions as a linearized voltage-controlled resistor and acts as a voltage to current conversion element. This implementation has the benefit of very high voltage-compliance, nearly up to the power supply rails. A cascoded current sources is used as

the reference current generator, and is shown in Figure 5.14. The current source also employs a gain-boosted cascode to increase output impedance (given by 5.4). This allows $V_{compliance}$ to be maintained across a range of currents. The source output impedance is given by 5.4,

$$R_{Out} = A_v g_{m\_cascode} r_{o\_cascode} R_{Triode\_FET} \tag{5.4}$$

In this design, the compliance voltage is set to V_{DD} – 100 mV, and is generated by the bandgap reference circuit described above. In order to keep the VCR in deep triode region, a $V_{GS} > V_{th}$ +200 mV. This is verified in simulation analysis, which yields a $V_{VCR\text{-}PMOS}$ = 800mV (V_{DD} = 3.1V, giving $V_{|SG|}$= 2.3V).

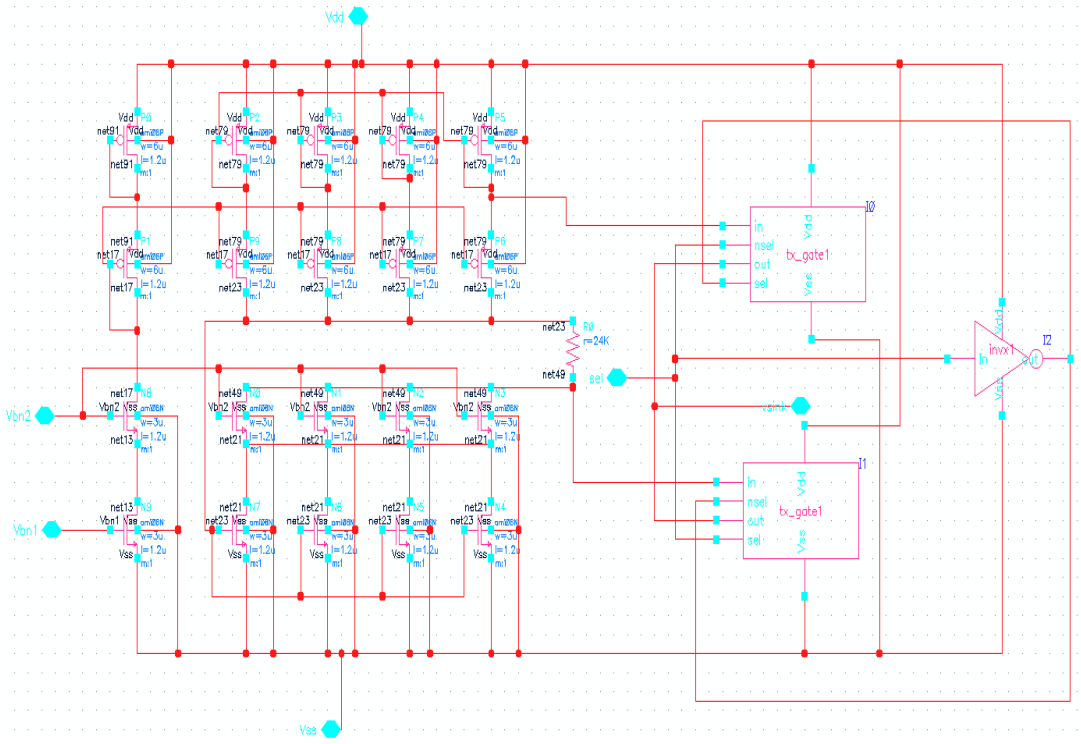


Figure 5.14: DAC Reference Current Source.

The gain-boosted cascode uses a 2-stage opamp shown in Figure 5.15. The opamp's AC response is shown in Figure 5.16. Mid-band Av is 48 dB, which (along

with the 96 /1.5 µm cascode maintain $V_{compliance}$ for source currents across the dynamic range of the source (20 µA – 3.3 mA).

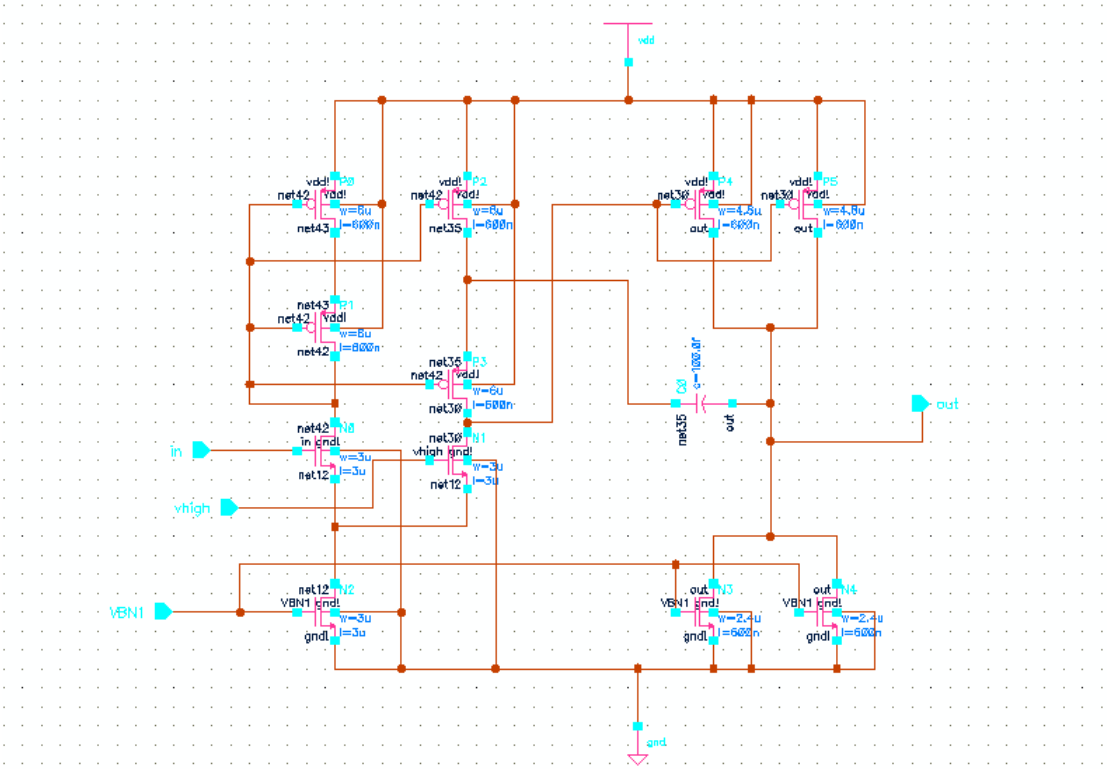


Figure 5.15: Amplifier for gain-boosting cascode circuit.

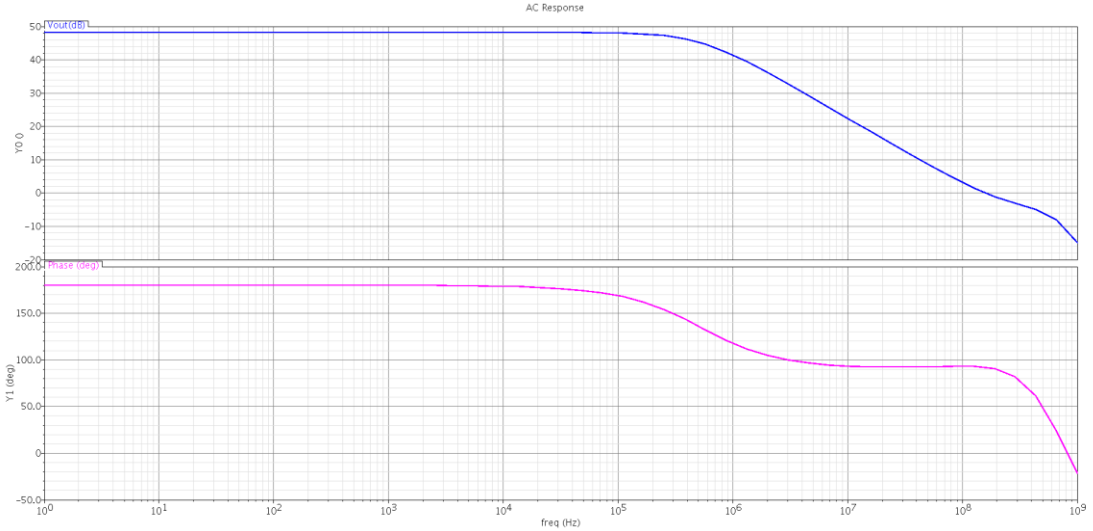


Figure 5.16: AC Response of Gain-boosting Cascode Operational Amplifier. Mid-band gain is 48 dB with 3 dB roll-off at 400 kHz.

The design of the current sink follows identical principles. $V_{compliance}$ is 892 mV from simulation and $V_{VCR\text{-}NMOS}$ is 2.1 V. Transient simulations of the Current

source and sink DACs across their range of operation are shown in Figures 5.17 (a) and (b) respectively. Figure 5.18 shows the overall DAC transfer function.

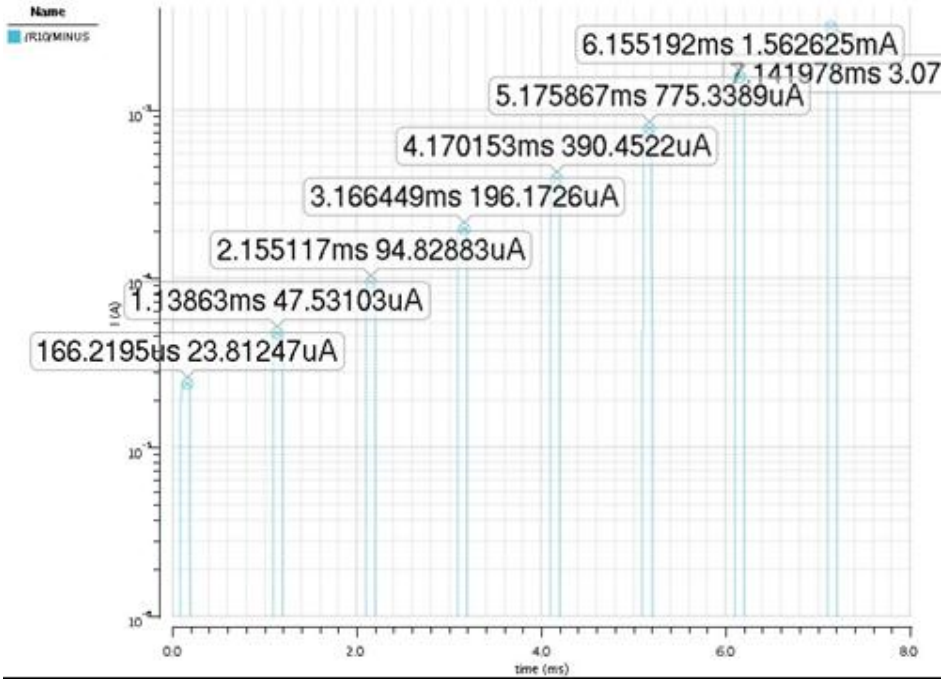


Figure 5.17 (a). Current Source output. Each current pulse is 100 µs wide and corresponds to an individual current-steering branch.

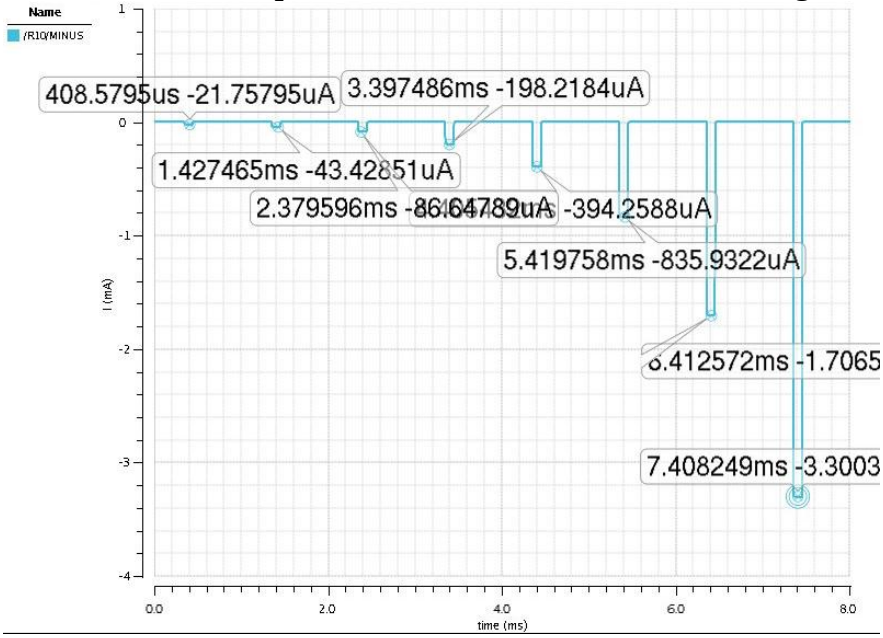


Figure 5.17 (b) Current Sink output. Each current pulse is 100 µs wide and corresponds to the digital code in the same way as described for 5.17(a).

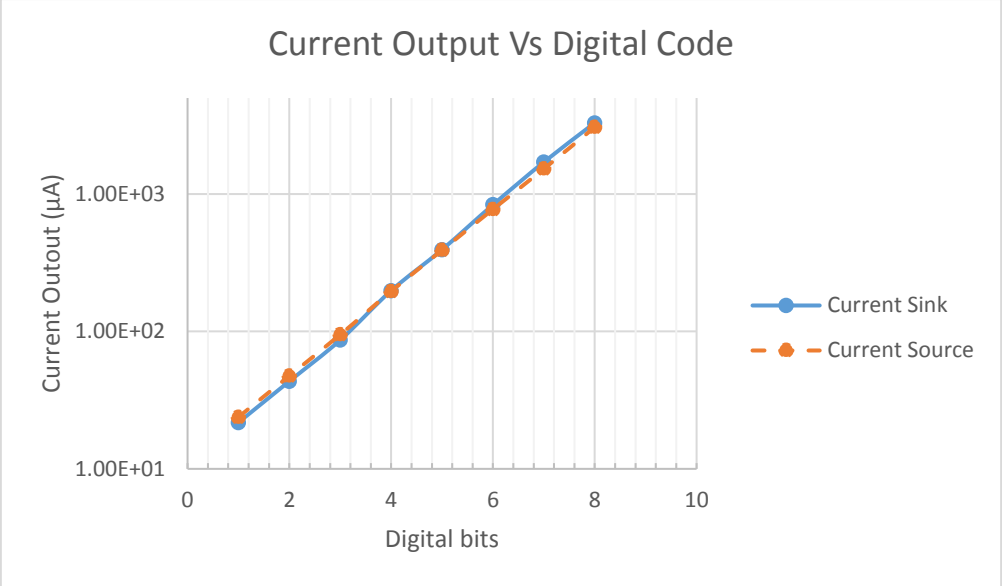


Figure 5.18: The Transfer function of 8-bit current source and sinks. The gain function source and sink are slightly mismatched, but this may be corrected through the digital code.

5.2.4 DAC Linearity

Both current source and sink DACs were found to be monotonic in simulation. While DAC linearity is not very important in the context of biological stimulation, a segmented DAC topology is particularly prone to non-linearities, which may impact the ability to charge-balance. Expected DAC non-linearity was thus characterized from simulation results 29]. The results are summarized in Table 5.3

SIMULATION	Current Source DAC	Current Sink DAC
LSB	23.81 µA	21.75 µA
Offset Error	101 nA	19 pA
Gain Error	0.86%	18.8%
DNL	Worst at I_{64} (-1.09 LSB)	Worst at I_{64} (+ 4.02 LSB)
INL	(+0.7, -0.45) LSB	(-2.35, +2.67) LSB

Table 5.3: Current Source and Sink Linearity from simulation

5.3 Fabrication and Testing

The microstimulation system was designed and fabricated in ON-SEMI 0.5µm CMOS process. Top level layout is shown in Figure 5.20. The full current source and sink occupied 400 µm x 350 µm, making it feasible to integrate them with a 16-channel amplifier chip. Control signals were issued by the digital controller implementation shown in Figure 5.21. The controller occupies 1500 µm x 350 µm. The entire chip is shown in Figure 5.22, and has a footprint of 2.5 mm x 3 mm.

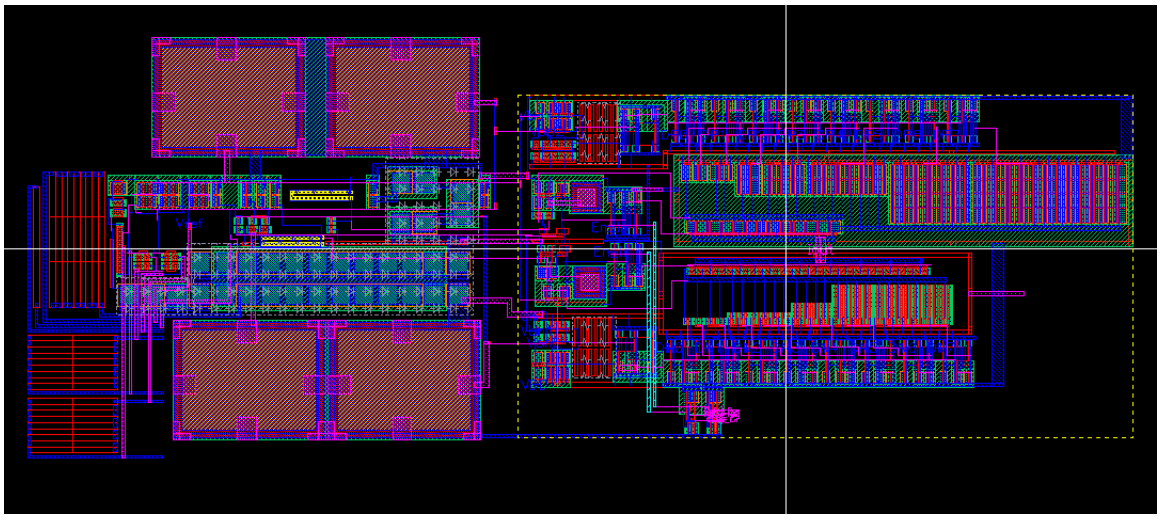


Figure 5.20: Current-Source and Sink Layout

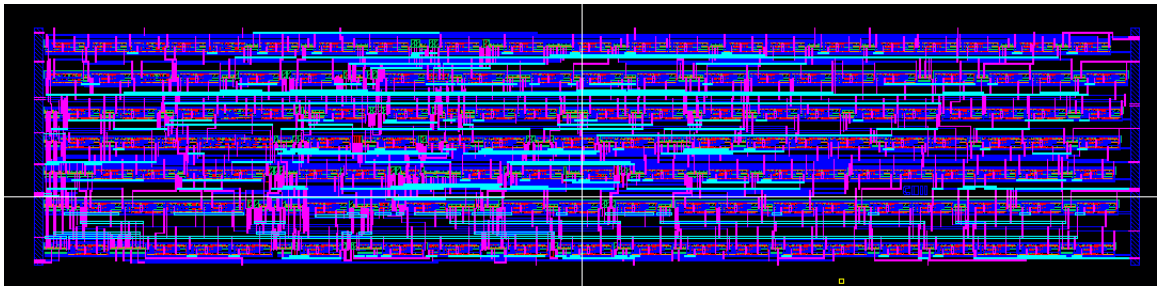


Figure 5.21: Digital Controller for 16-channel Stimulation Chip

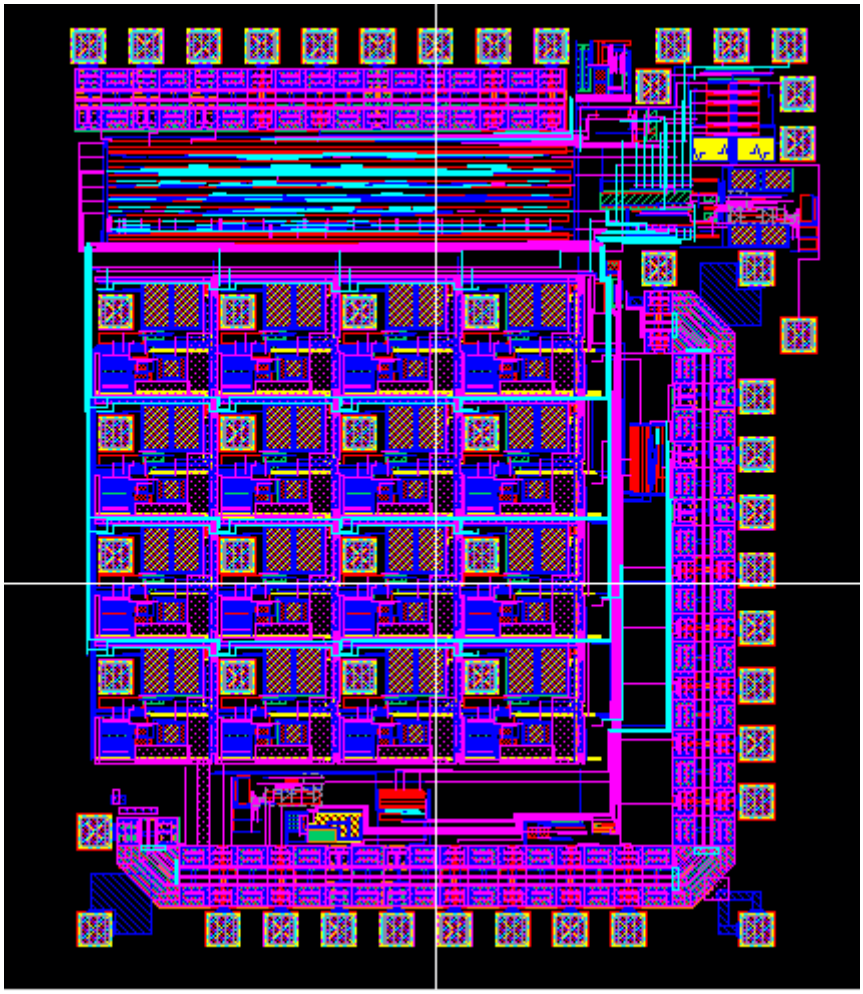


Figure 5.22: 16 channel- amplifier chip with 8-bit stimulation source

The current source transistors were designed with multiple fingers to im prove matching and dummy transistors were added to shield from edge effects. All p-transistors were laid out in the same n-well and the DAC was provided an isolated power supply lime to prevent coupling from the clock line. A photomicrograph of the fabricated ASIC is shown in Figure 5.23.

The ASIC was testing on benchtop, and Figure 5.24 demonstrates a representative biphasic current pulse.

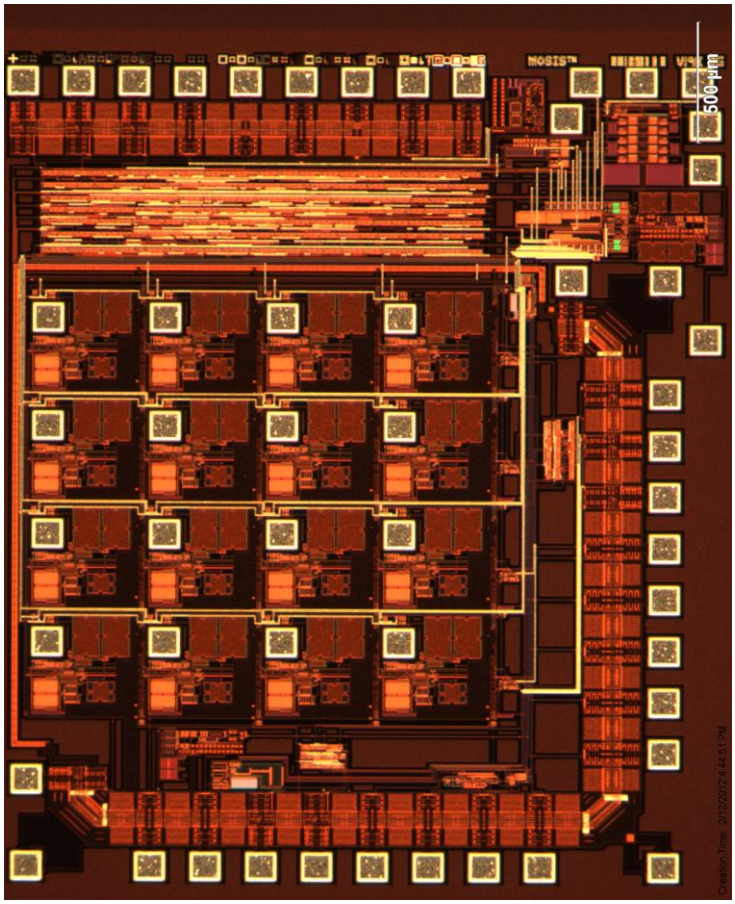


Figure 5.23: Photomicrograph of 16-channel amplifier chip with Current source

The dynamic range of the DACs were tested and a linearity analysis of the bench top measurements was completed. The transfer function of the source and sink DACs are shown in Figure 5.24. Linearity Analysis results are summarized in Table 5.6.

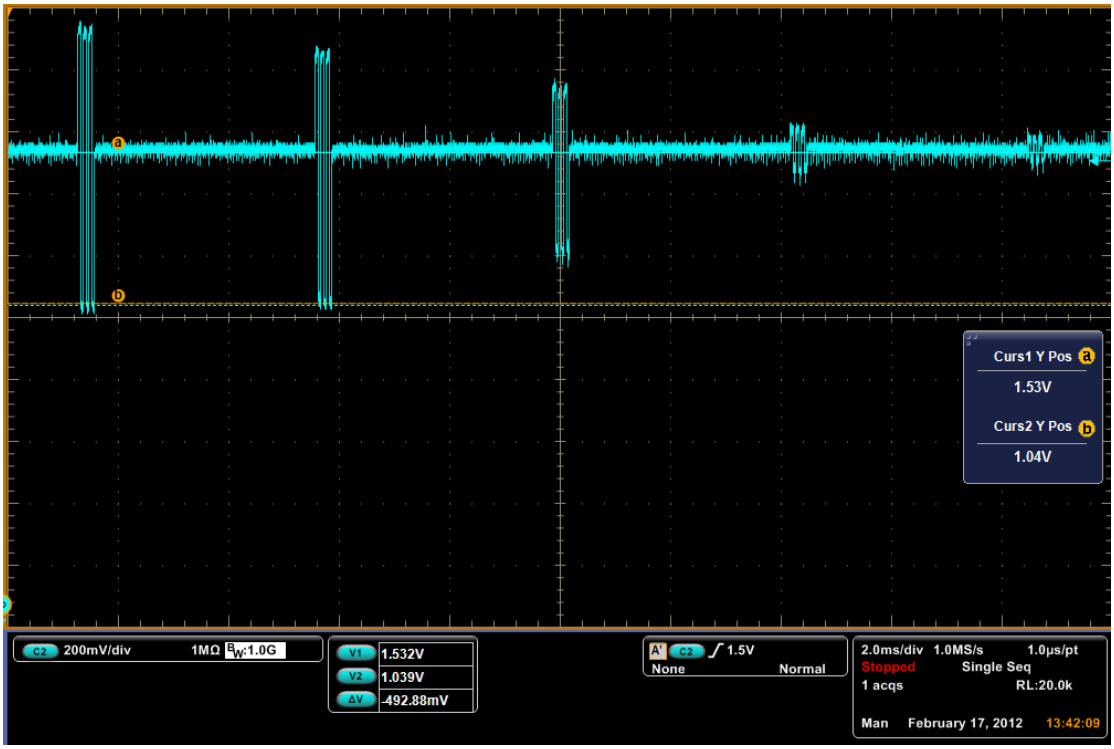


Figure 5.24: Oscilloscope capture from bench top testing of 16-channel stimulation chips showing bipolar pulses with ramping current magnitude.

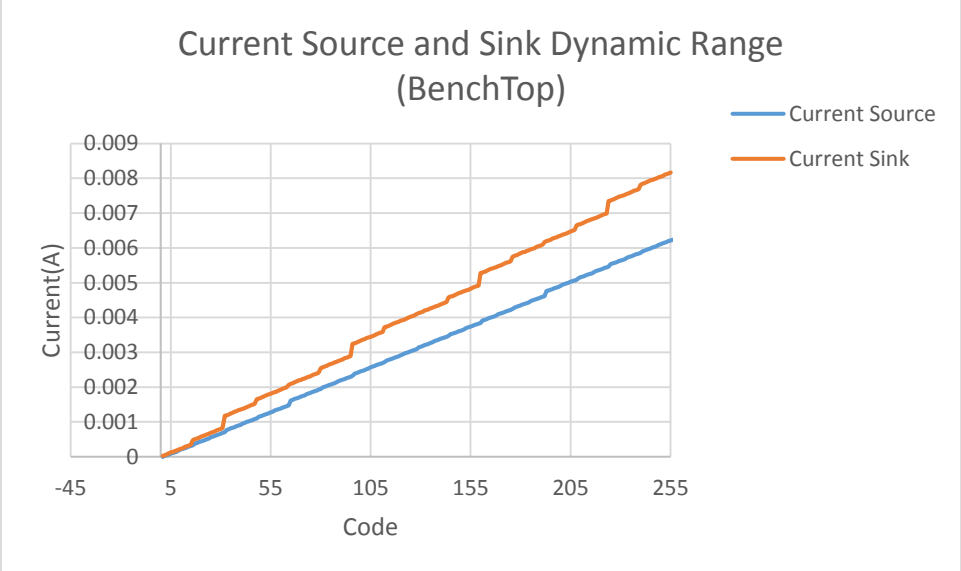


Figure 5.25: Source and Sink DAC Transfer function from bench top tests

BENCHTOP	Current Source DAC	Current Sink DAC
LSB	20.8 μA	24.3 μA
Offset Error	Not measurable	Not measurable
Gain Error	17.45%	31.68%%
DNL	Worst at I_{64} (+5.0 LSB)	Worst at I_{32} (+ 9.97 LSB)
INL	(+2.3,-1.9) LSB	(+4, -4.2) LSB

Table 5.6: Linearity Analysis from Benchtop Data

Bench top testing of the stimulation source was able to verify its dynamic range. Generation of biphasic current sources with user-programmed features was also validated. Linearity testing has revealed moderate non-linearities, worse with the Sink DAC than the Source DAC. The stimulation ASIC could nonetheless be utilized as a current source after linearity calibrations. Next steps will involve building a test system the stimulation system for more thorough testing and verification in bench-top and in-vitro tests.

5.4 References

1. Deep-Brain Stimulation for Parkinson's Disease Study Group. "Deep-brain stimulation of the subthalamic nucleus or the pars interna of the globus pallidus in Parkinson's disease." The New England journal of medicine 345.13 (2001): 956.

2. Coubes, Philippe, Laura Cif, Hassan El Fertit, Simone Hemm, Nathalie Vayssiere, Stephanie Serrat, Marie Christine Picot et al. "Electrical stimulation of the

globus pallidus internus in patients with primary generalized dystonia: long-term results." Journal of neurosurgery 101, no. 2 (2004): 189-194.

3. Plow, Ela B., and Andre Machado. "Invasive neurostimulation in stroke rehabilitation." Neurotherapeutics 11, no. 3 (2014): 572-582.

4. Levy, Robert, Sean Ruland, Martin Weinand, David Lowry, Rima Dafer, and Roy Bakay. "Cortical stimulation for the rehabilitation of patients with hemiparetic stroke: a multicenter feasibility study of safety and efficacy." (2008).

5. Ranck, James B. "Which elements are excited in electrical stimulation of mammalian central nervous system: a review." Brain research 98.3 (1975): 417-440.

6. Rattay, F. "The basic mechanism for the electrical stimulation of the nervous system." Neuroscience 89.2 (1999): 335-346.

7. Luan, Song, Ian Williams, Konstantin Nikolic, and Timothy G. Constandinou. "Neuromodulation: present and emerging methods." Frontiers in neuroengineering 7 (2014).

8. Merrill, Daniel R., Marom Bikson, and John GR Jefferys. "Electrical stimulation of excitable tissue: design of efficacious and safe protocols." Journal of neuroscience methods 141.2 (2005): 171-198.

9. Dymond, Anthony M. "Characteristics of the metal-tissue interface of stimulation electrodes." Biomedical Engineering, IEEE Transactions on 4 (1976): 274-280.

10. Cogan, Stuart F. "Neural stimulation and recording electrodes." Annu. Rev. Biomed. Eng. 10 (2008): 275-309.

11. Tehovnik, Edward J. "Electrical stimulation of neural tissue to evoke behavioral responses." Journal of neuroscience methods 65.1 (1996): 1-17.

12. Ghovanloo, Maysam. "Switched-capacitor based implantable low-power wireless microstimulating systems." In Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on, pp. 4-pp. IEEE, 2006.

13. Rosellini, W. M., Yoo, P. B., Engineer, N., Armstrong, S., Weiner, R. L., Burress, C., et al. (2011). A voltage-controlled capacitive discharge method for electrical activation of peripheral nerves. Neuromodulation 14, 493–499.

14. Miocinovic, Svjetlana, and Warren M. Grill. "Sensitivity of temporal excitation properties to the neuronal element activated by extracellular stimulation." Journal of neuroscience methods 132, no. 1 (2004): 91-99.

15. McCreery, Douglas B., William F. Agnew, Ted GH Yuen, and Leo Bullara. "Charge density and charge per phase as cofactors in neural injury induced by electrical stimulation." Biomedical Engineering, IEEE Transactions on 37, no. 10 (1990): 996-1001.

16. Stern, Shani, Andres Agudelo-Toro, Assaf Rotem, Elisha Moses, and Andreas Neef. "Chronaxie Measurements in Patterned Neuronal Cultures from Rat Hippocampus." PloS one 10, no. 7 (2015): e0132577.

17. Moro, E., R. J. A. Esselink, J. Xie, M. Hommel, A. L. Benabid, and P. Pollak. "The impact on Parkinson's disease of electrical parameter settings in STN stimulation." Neurology 59, no. 5 (2002): 706-713.

18. Grill, Warren M., and J. Thomas Mortimer. "Stimulus waveforms for selective neural stimulation." Engineering in Medicine and Biology Magazine, IEEE 14.4 (1995): 375-385.

19. Sahin, Mesut, and Yanmei Tie. "Non-rectangular waveforms for neural stimulation with practical electrodes." Journal of neural engineering 4.3 (2007): 227.

20. Brown, Edgar A., James D. Ross, Richard A. Blum, Yoonkey Nam, Bruce C. Wheeler, and Stephen P. DeWeerth. "Stimulus-artifact elimination in a multi-electrode system." Biomedical Circuits and Systems, IEEE Transactions on 2, no. 1 (2008): 10-21.

21. Gnadt, James W., et al. "Spectral cancellation of microstimulation artifact for simultaneous neural recording in situ." Biomedical Engineering, IEEE Transactions on 50.10 (2003): 1129-1135.

22. Blum, Richard A., et al. "Models of stimulation artifacts applied to integrated circuit design." Engineering in Medicine and Biology Society, 2004. IEMBS'04. 26th Annual International Conference of the IEEE. Vol. 2. IEEE, 2004.

23. Nag, Sudip, et al. "Sensing of stimulus artifact suppressed signals from electrode interfaces." Sensors Journal, IEEE 15.7 (2015): 3734-3742.

24. Bertotti, Gabriel, et al. "A CMOS-based sensor array for in-vitro neural tissue interfacing with 4225 recording sites and 1024 stimulation sites." Biomedical Circuits and Systems Conference (BioCAS), 2014 IEEE. IEEE, 2014.

25. DiSpirito, Hailey, et al. "A Neural Stimulation System Model to Enhance Neural Integrated Circuit Design." Biomedical Engineering Conference (SBEC), 2013 29th Southern. IEEE, 2013.

26. M. Ghovanloo and K. Najafi, "A compact large voltage compliance high output impedance programmable current source for biomedical implantable microstimulators," IEEE Trans. on Biomed. Eng., vol. 52, no. 1, pp. 97–105, Jan. 2005.

27. Buller, J. F., J. Fletcher, S. Meyers, M. Robinson, F. Tamayo, A. Prakash, and D. Cabler. "Band-gap circuit design challenges in high-performance 32-nm technology." In Custom Integrated Circuits Conference (CICC), 2011 IEEE, pp. 1-4. IEEE, 2011.

28. Bastos, Jose, et al. "Matching of MOS transistors with different layout styles." Microelectronic Test Structures, 1996. ICMTS 1996. Proceedings. 1996 IEEE International Conference on. IEEE, 1996.

29. David Fry. Adjusting and Calibrating Out Offset and Gain Error in a Precision DAC. https://www.maximintegrated.com/en/app-notes/index.mvp/id/4602

30. Pelgrom, Marcel JM, Aad CJ Duinmaijer, and Anton PG Welbers. "Matching properties of MOS transistors." IEEE Journal of solid-state circuits 24.5 (1989): 1433-1439.

31. ON-SEMI C5F/N Design Kit. Obtained through MOSIS.

32. Gupta, Shantanu. "CURRENT STEERING D/A CONVERTER W-2W DAC & Programming Resistive Memory." Accessed on March 23rd,2016. http://www.cmosedu.com

Chapter 6. Future Directions and Conclusion

The ASIC implementations of the Impedance Spectroscopy and Stimulation functionalities described in this work are incremental steps toward the realization of a multi-modal, closed-loop, implantable neuroprosthetic device. The neural recording platform that these features are integrated on to are described in detail in Chapter 2, and comprise three ASICs (for signal amplification, digitization and transmission respectively as described in Chapter 3). Analog to Digital signal conversion on these systems, however, is still performed using off-the-shelf ADCs from Linear Technologies. The natural next step toward large-scale integration is the incorporation of the ASICs described above long with custom ADCs onto a single IC platform. This offers many benefits from the perspective of area and power savings, and would optimize signal to noise ratio. An engineering analysis of the scope of this redesign exercise, as a first step toward pursuance of this SoC endeavor, is outlined in the first part of this Chapter.

The vision of a neural prosthesis that extends beyond the constraints of a rigid multielectrode array are being increasingly discussed in BCI literature [1]. The implementation of such a distributed network of self-sufficient, independent nodes is a major paradigm shift, and requires an in-depth analysis of the design space and limitations. This is described in the latter half of this chapter.

The design discussions highlighted in this chapter provide a summary of the major lessons learned from the development of these devices. Finally, I conclude this Chapter with reflections on the contributions of the novel elements of this work on these device projects as well as the greater field of implantable neural prosthetic systems.

6.1 System on Chip (SoC) Approach for a Multi-modal ASIC for a Closed- Loop Neural Prosthetic System

The neural recording platforms described in Chapter 2 are presently undergoing translational efforts into the clinical domain. ASIC characterizations, verifications and documentation as they pertain to this exercise are addressed in Appendix I. An integral part of the future development plan for these systems is the implementation of a System on Chip (SoC) ASIC, integrating signal amplification and digitization (including Analog to Digital Conversion) on the same silicon chip. The performance specifications for this SoC ASIC are derived from both personal experience at Brown, as well as a survey of reports and strategies described in recent electronics and neuroengineering literature. This mandates careful consideration of the step-wise evolution of the current design and architecture, and the lessons learned therein. Figure 6.1 provides an overview of the multimodal functionality to be integrated on the SoC ASIC.

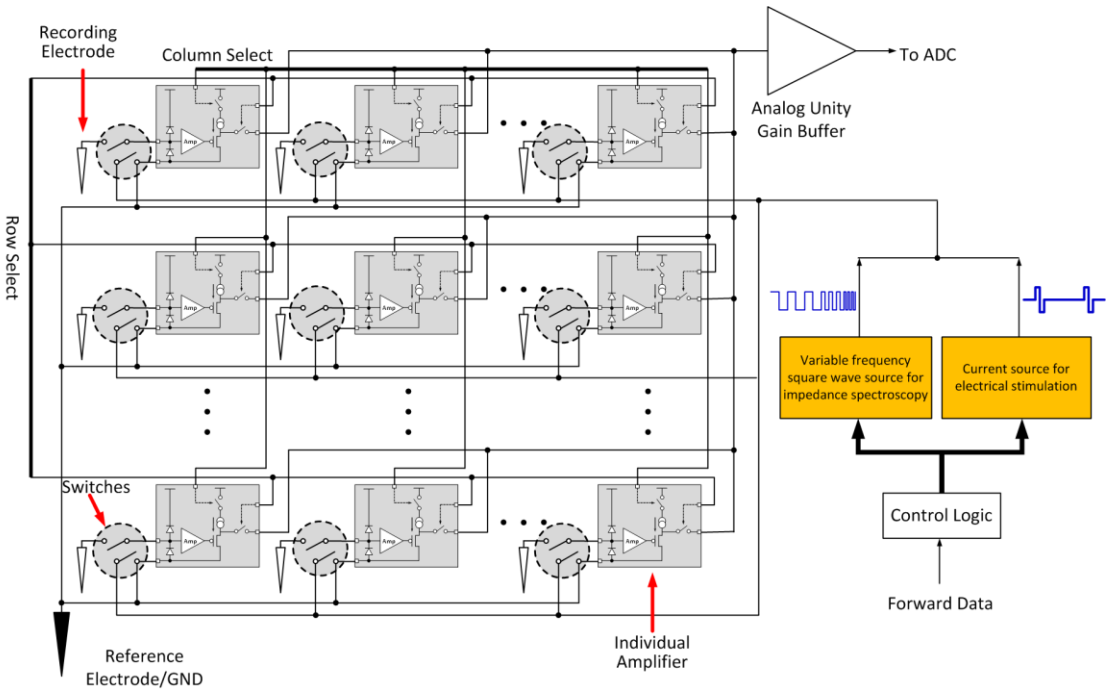


Figure 6.1: Overall Multimodal Architecture of the SoC Analog-Front End with Recording, Impedance Spectroscopy and Biphasic Stimulation functionalities.

Figure 6.2 (a- d) further elaborates on each of these individual functions to be accomplished by this ASIC. This architecture and design, conceived at Brown, is expected to be implemented through a collaborative endeavor with industry partners, and a comprehensive analysis of the approach is described below:

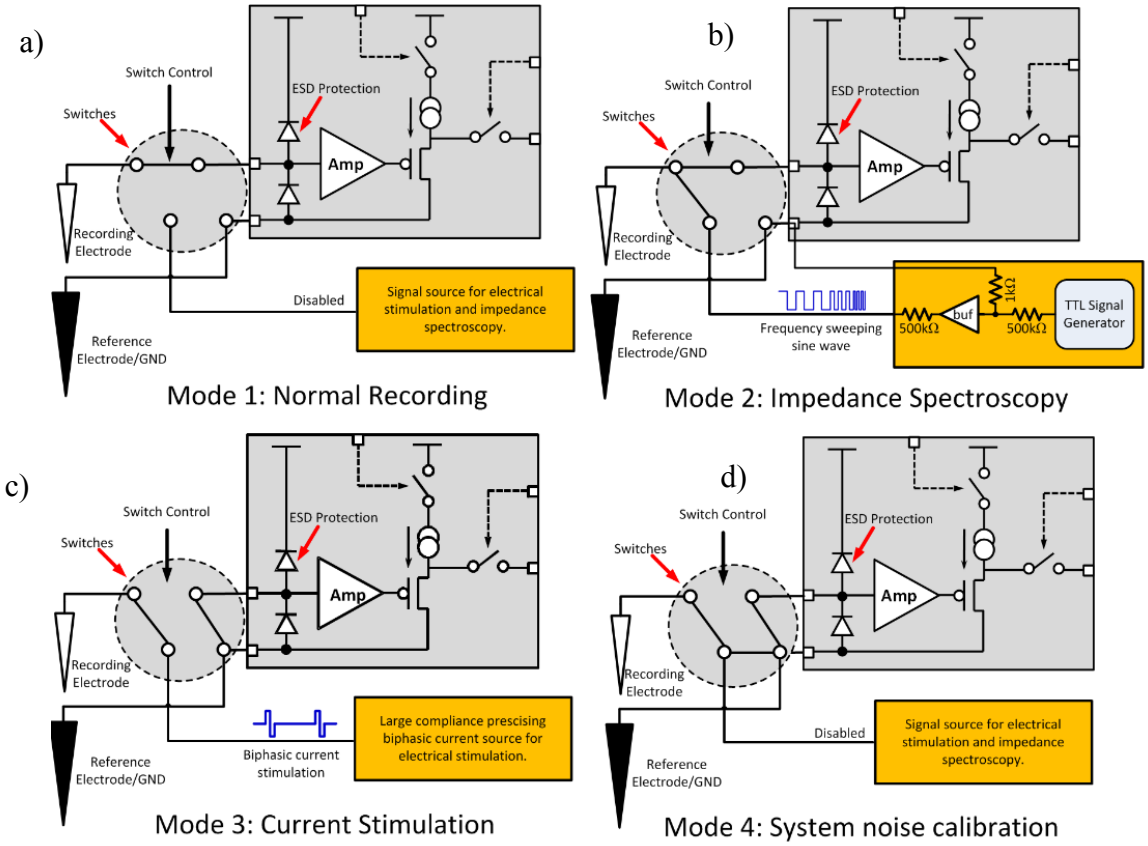


Figure 6.2: System Configurations for the multi-modal SoC. (a) (Top Left) Recording mode: All other subsystems disabled. (b) (Top Right) Impedance Spectroscopy mode: AC Voltage Source enabled while amplifier measures impedance response. (c) (Bottom Left) Stimulation mode: Current Source/Sink enabled and amplifier at stimulation site connected to ground. (d) Discharge mode: may be used between stimulation pulses or for System Noise calibration mode. All Amplifiers are connected to ground.

6.1.1 Power, Area and CMOS Process

The current CMOS technology of choice for the implementation of the neural amplifier and digitization Controller ASIC is ON-Semiconductors' 0.5µm C5F/N process. The RF transmitter is implemented using the IBM 7WL BiCMOS process, but since the latter is not part of the first generation SoC design, it will be left out of further discussions in this Chapter. The original choice of CMOS process for the amplifier and controller ASICs was driven by a number of factors, not trivial among

which were ease of access to academic multi-project run wafers through MOSIS as well as optimized silicon cost per area given the particular system topology. For example, the architectural choice for the Amplifier ASIC is a design with a 400 μm x 400 μm footprint for each individual channel to allow for direct integration with the microelectrode array. A large fraction of the amplifier's area (approximately 60%) is occupied by the input transistors and the feedback capacitors to optimize for low-frequency noise and amplifier mid-band gain respectively. Nonetheless, an optimized design readily fits into the assigned area budget, even in the rather dated 0.5 μm process. The latter, due to its age, happens to also be the most economical fabrication option, and is thus chosen for this work.

The integration of ADCs onto a SoC platform is area intensive and mandates revisiting the CMOS process discussion. Bulk CMOS processes at 180 and 350 nm have been staples in the biomedical ASIC industry over the last decade with many reports of successful ADC designs with 12-14 bit resolution [4, 5]. The potential to operate at lower supply power (1.1V, 1.5 V and 1.8 V being some options) is also an enticing option for an implantable device. SoC design in a process technology different from our current implementation would involve the translation of current ASICs to the new process (in a scaling exercise similar to that described in Chapter 3). The relative difference between the device parameters in these two processes determines the amount of effort expended in the translation (versus complete redesign) to maintain matching chip performance specs. The argument for power and area savings for a System on Chip are however extremely compelling, leading to the choice of the 180 nm bulk CMOS process for the SoC implementation.

6.1.2 Neural Probe for Bidirectional Neuroprosthetic Applications.

The Intracortical microelectrode array platform utilized in our implantable systems comprises micromachined silicon probes with platinized tips. Probe impedances typically range from 100-600 kΩ, with nominal values of 100 kΩ. Physiologically significant electrical stimulation requires 10s-100s μA to be delivered to tissue. This is a task fundamentally incompatible with the above-mentioned probes if compliance voltages are to be kept within reasonable range. An alternative, lower impedance neural probe is thus an essential requirement for a closed-loop neuroprosthetic system. Activated or Sputtered Iridium Oxide (AIROF and SIROF respectively) based microelectrodes are one such option, and will likely be the probe of choice for the next generation closed loop devices. Figure 6.3 depicts the impedance response of the IrOx Utah MEA. Impedances at 1 kHz are at least one order of magnitude smaller when compared with corresponding Platinum electrodes.

Probe impedance is a direct determinant of electrode thermal noise, which in turn is a critical specification for system electronic design. A lower-impedance, less-noisy probe thus impacts the overall design in the several ways, which are individually addressed in their respective sub-sections below.

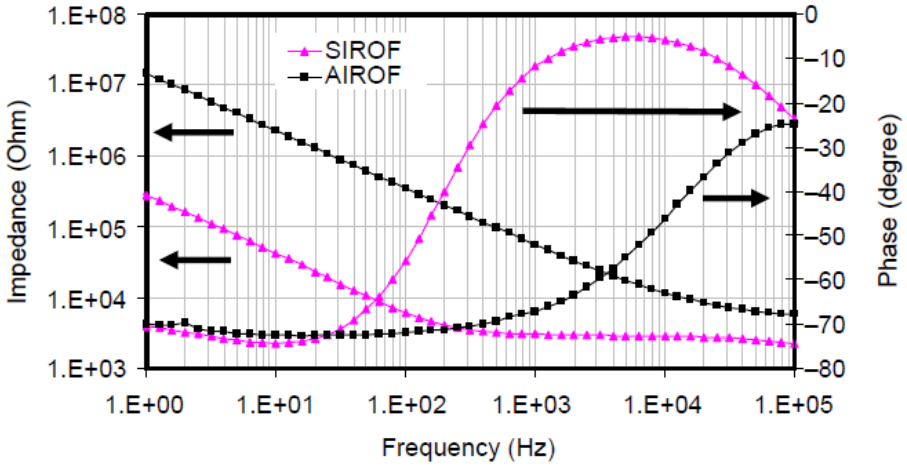


Figure 6.3: Impedances (Magnitude and Phase) of Iridium Oxide Electrodes. Sputtered Iridium Oxide (SIROF) devices at 1 kHz have impedances in the 10-50 kΩ range. From [2].

6.1.2A Neural Amplifiers

The numbers of publications describing neural recording ICs has steadily increased over the last decade [5-10]. The basic design topology of the neural amplifier has remained largely unchanged and is characterized by:

i. High-gain operational transconductance amplifier

ii. Low-pass cutoff frequency between 7-10 kHz.

iii. AC coupled inputs with DC rejection achieved through implementation of a feedback RC high-pass filter.

iv. A pseudo-resistor implementation (with resistances in GΩ range) to push the high pass cutoff frequency described by (iii) in the 0.1-100 Hz.range.

v. Low-noise, ideally limited by the thermal noise of the neural probe.

While the over-arching principles of amplifier design remain unchanged for the SoC, the 10x reduction in probe impedance would lead to a corresponding reduction in RMS thermal noise, which sets the upper bound for amplifier electronic noise. This in turn, would directly impact transistor sizing (particularly input transistor size) for a proportionally lower amplifier noise.

6.1.2B Analog to Digital Conversion

The commercial 12-bit ADCs utilized in the current device have a sampling rate of 1.5 MSamples/second and an SNR of 73 dB [11]. Power consumption from a 3.0 V supply is 4.8 mW each (making the ADC the most power-hungry component on the entire system). A custom ADC design would enable speed vs power consumption optimization, and is thus a desirable goal for a neural prosthetic SoC ASIC. This trade-off depends on ADC architecture and is extensively discussed in literature and the depicted in Figure 6.4 below.

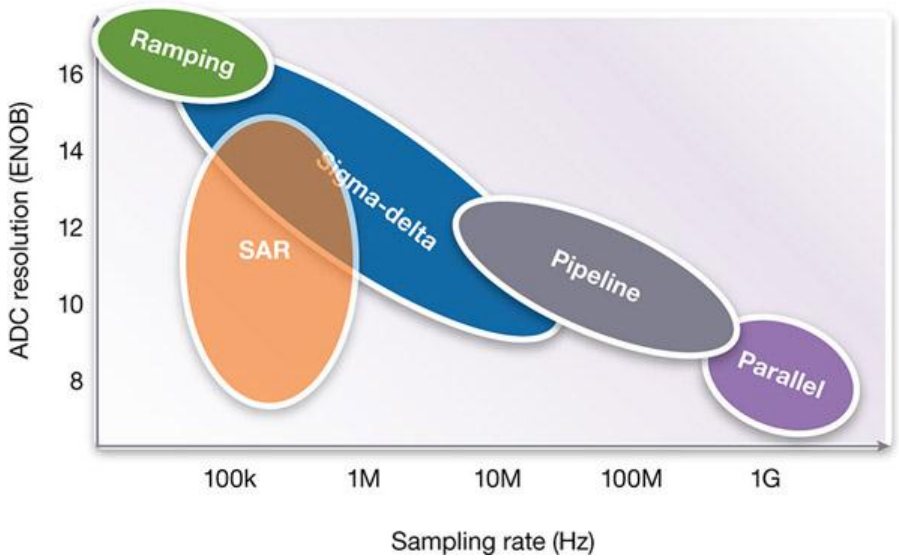


Figure 6.4: ADC Sampling Rate vs Resolution for major well-established architectures.

The numbers for a neural recording application are mid- spectrum in Figure 6.4. ADC bit resolution specification for neural recordings, driven by the quantization noise limit, is adequate in the 12-14 bit range even after taking into account the thermal noise reduction from IrOx electrodes. A channel sampling rate of 20kSamples/second based on Nyquist theory, and a total channel count is in the 100-128 range is chosen for compatibility with the Utah MEA. A single ADC for the above-described system thus needs to have a sampling rate of approximately 3MSamples/second. Based on Figure 6.4 above, Successive Approximation Register (SAR) and Sigma-Delta Converters (σΔ) are the two optimal ADC architectures choices in the identified performance range. SAR ADCs are significantly more power-efficient, and this would thus be the architecture of choice for SoC implementation.

6.1.2C Digital Control

The current Digital Controller chip addresses the data multiplexing and packaging needs for the recording system. The impedance spectroscopy and stimulation ASICs have their own digital modules to address their data processing needs. Each of these is implemented in Hardware Description Language (HDL) and can seemlesslybe ported into the 180 nm technology via re-synthesis. The SoC Controller block would integrate all digital processing needs of these modules onto a single digital engine.

6.1.2D Stimulation and Impedance Spectroscopy Analog Modules

The impedance spectroscopy module relies on a digital source waveform, and may thus be migrated with relative ease. The stimulation current sources and sinks DACs, however, would have to undergo extensive changes in the scaling exercise (similar to the amplifiers). The final specifications for stimulation circuitry design, derived from the design exercise and matching considerations described at the end of Chapter 6 are:

i. Single Current Source with switchable directionality, as described in Figure 6.5 for improved charge balance.

ii. Current Amplitudes from 1 μA to 1mA

iii. Biphasic Stimulation, with independent control over pulse width in each phase

iv. Control over a programmable inter-phase interval between the cathodic and anodic pulse phases

v. Programmable frequency and pulse trains.

The SoC project, guided by the design principles described above, is expected to deliverable over the next 12-18 months.

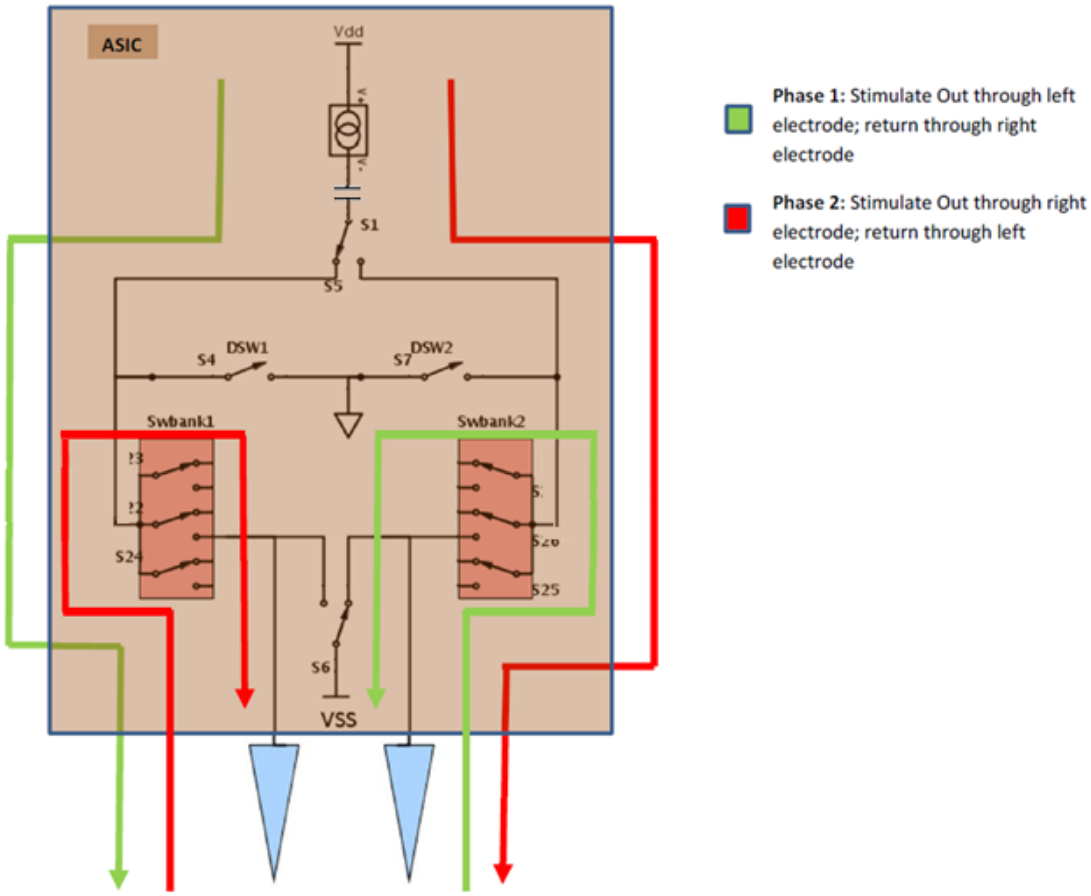


Figure 6.5: A single source biphasic pulse generator for improved matching

6.2 Single Channel ASIC Pay-load for a Distributed Sensor Network Node

Multi-channel neural recording platforms of the type described in this thesis have advanced our scientific understanding of neural population dynamics in many profound ways. These bulky implants however face several challenges due to their size and tethering constraints. It is also difficult to access certain anatomical locations such as deep gyri in a meaningful way. The brain performs multi-dimensional integration; a realistic neuroprosthetic device should have the capacity to

the same. This is a daunting task, which becomes rapidly unattainable given current technology paradigms focusing on single-platform implants. Truly "wireless" front-end units with distributed data acquisition and processing need to be envisioned if we are to push past the technological limits posed by the current bulky implants. An approach to the design of such units is described below:

6.2.1 System Specifications

The migration from a single-platform integrated system to a distributed sensor network approach may be achieved by developing extremely miniaturized (100-200 μm) individual sensors that are self-reliant in terms of power and telemetry. At this size, these individual units may be deployed to various brain foci using injection delivery mechanisms. From a materials perspective, the hermeticity requirement is still the same (which may be satisfied using glass-based packaging for active electronics). The electronics payload within each unit needsto fulfil the same specifications as an individual channel on the integrated platform described earlier in this document, and summarized below:

i. *RF power:* For this topology and at the above-mentioned scale, each sensor unit needs to rely on harvested RF power from a remote RF transmission source for full operation.

ii. *Neural Signal Probe and Amplifiers*: Pure, highly-conductive metals such as gold may be used to serve as a miniature, biocompatible neural probes. MicroElectroMechanical Systems (MEMS) techniques enabling gold feedthroughs in ceramic/glass packages have been described in literature and would be an appropriate

to use here. Each sensor needs its own ASIC—the signal acquisition and amplification performance needs would remain unchanged from the present system.

iii. *Signal processing and Digitization*: Power and data bandwidth needs make it impractical to perform broadband signal acquisition. Data compression through spike detection is thus a necessity for this type of sensor implementation, and is discussed in greater detail below. A standard approach of spike counting and bin-count transmission at a low frequency (20 ms bins with 50Hz transmission as a typical example) could be implemented. Each packet would additionally need one full digitized sample for calibration of spike detection thresholds, requiring the implementation of a 6-10 bit ADC.

iv. *Telemetry*: This is an important consideration. Data compression from (iii) would mitigate the power needs for outgoing telemetry in an individual node. A passive RF backscatter modulation scheme may provide further power savings. The ability to have reliable incoming telemetry (to enable stimulation, for example) is very important. This requires the implementation of a receiver/decoder module. Additionally, it poses an important systems level constraint mandating that each node be individually and statically addressable. The latter is also a crucial requirement from the perspective of longitudinal learning in the extra-cortical signal processing modules.

v. *Stimulation*: Harvesting adequate ambient RF power to produce the voltages needed for effective stimulation is not a feasible option, thus mandating implementation of a charge pump for voltage augmentation. Stimulation current

delivery may be further optimized through adiabatic charge balancing approaches [13, 14].

Most critically, the features outlined above need to be implemented in100 µm x 100 µm area of silicon real-estate. Power dissipation of an individual sensor must also remain firmly within the guidelines for prevention of tissue damage, which sets the limits at 10s of µW at this scale. The realization of a sensor node meeting these specs is highly ambitious, requiring exploration of cutting-edge FDSOI or FINFET technologies optimized for RF performance. The area constraints for the device may additionally require three-dimensional stacking of ICs, as demonstrated in the overview diagram of a single-channel sensor in Figure 6.6.

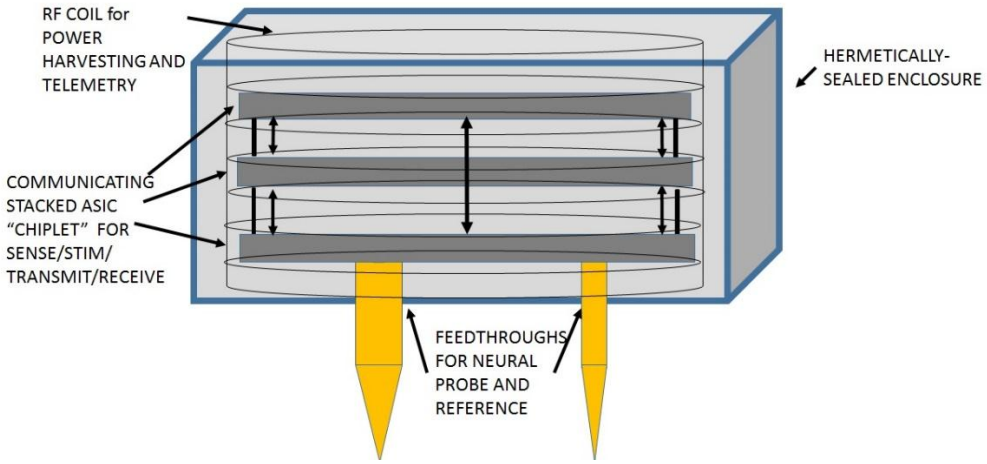


Figure 6.6: An individual hermetically sealed glass-packaged neural sensor with stacked ICs and RF power harvesting/telemetry

6.2.2 Power-Efficient ADCs and Spike Detection Approaches

Implementing a system with the stringent power-consumption specs described above cannot be achieved without detailed attention to the most power-intensive blocks. Optimizing ADC power is of particular importance and is thus discussed here. Figure 6.7 shows a sampling of low-power ADCs reported in literature:

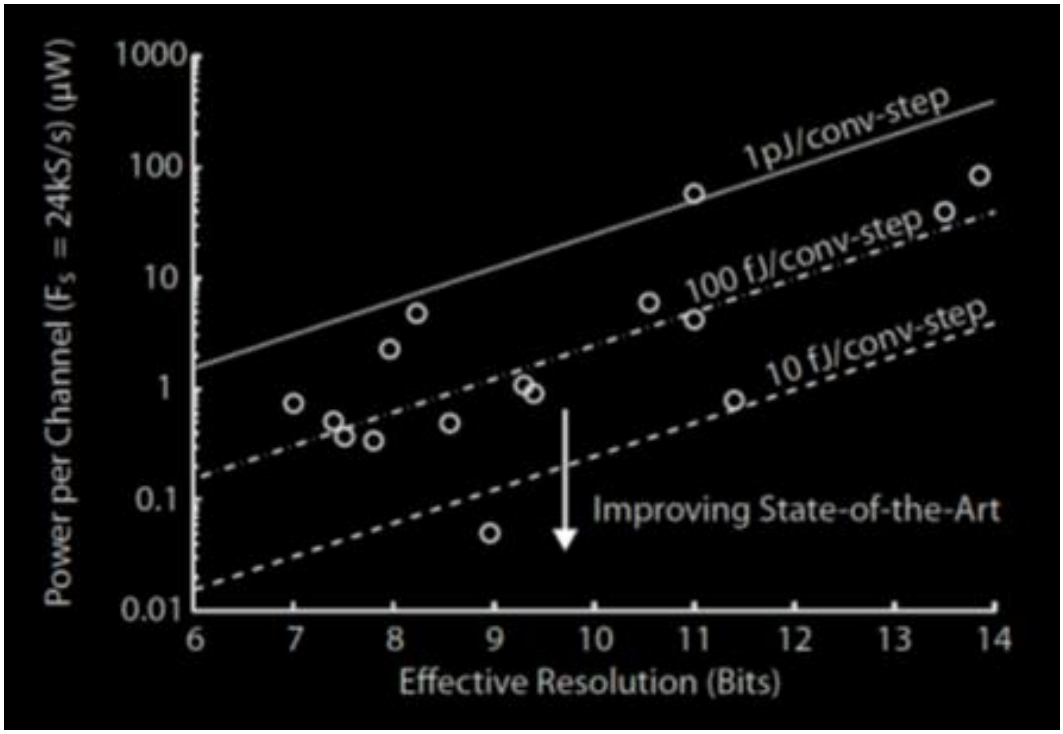


Figure 6.7: ADC power consumption vs Effective bit resolution. From [15]

The most important thing to note in Figure 6.7 is that ADCs with high Figure of merit (10-100 fJ/conversion-step) and ENOB between 7-9 bits with sub microwatt single channel power-consumption have been described in literature, and are possible to implement for the neural sensor node with careful CMOS process selection and design.

All previous prototype systems developed in our group have utilized broadband data transmission. While we have limited experience with data compression schemes, a wide variety of analog and digital data compression strategies have been reported in literature [15-26]. Digital and hybrid schemes using on-chip logic circuitry such as multipliers and large buffers are precluded from consideration due to the tight space constraints of a 100 μm sensor footprint. Analog spike detection strategies employ fewer components and are thus more compatible with the microminiaturized single node specifications. A basic spike detection circuit is

depicted in Figure 6.8 (and originally described in [15]). This spike detector design relies on 2 components: an RMS noise calculator a thresholding comparator (where the latter may be user-programmable). Threshold crossings are then simply aggregated and reported as a bin-count.Such latched comparator-based absolute-voltage thresholding implementations have been reported in literature [24] with power consumptions <1uW and areas between 0.021-0.24 mm2 and are thus feasible approaches for our single-channel implementation.

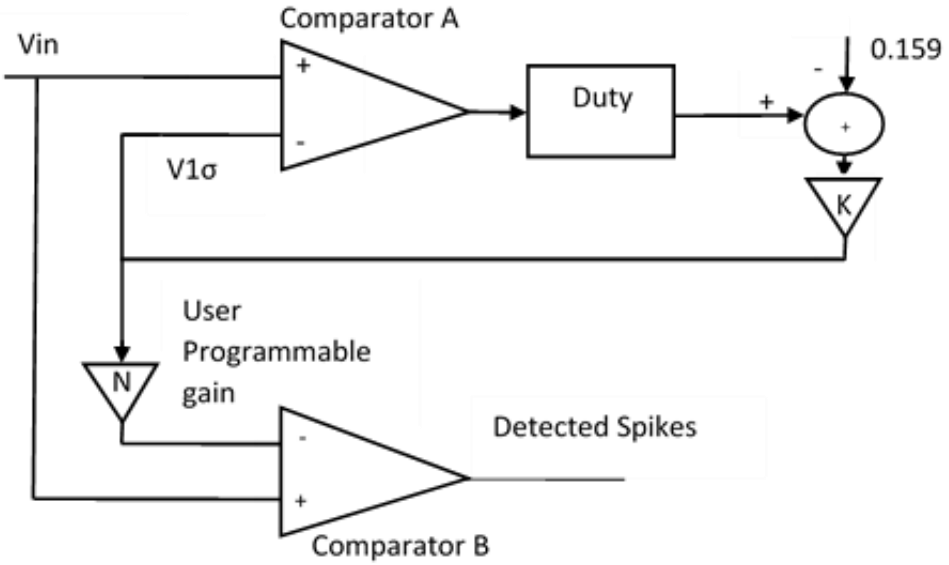


Figure 6.8: Latched Comparator-based Analog Spike Detection Circuit. Comparator A forms part of a proportional feedback controller, which is able to determine the $V_{1\sigma}$, the RMS value of V_{in} (assuming a Gaussian distribution with zero mean). N serves as a User-programmable multiplier for adaptive thresholding. Comparator B is then triggered each time V_{in} crosses the spike detection threshold.

6.3 Conclusion

This works described in this thesis span a range of neuroengineering contributions from individual integrated circuit design to wireless implantable system design and testing. Major novel contributions from the works highlighted herein are the development of a multimodal system with the addition of impedance spectroscopy and patterned biphasic current stimulation to a low-power, low-noise neural sensing platform. This type of multi-channel recording platform incorporating both impedance spectroscopy and stimulation has not been described in literature yet, and offers a tremendous opportunity to both better probe the dynamic characteristics of implant biophysics and provide a mechanism for closed loop feedback control of neural prosthetics.

Characterization of the impedance spectroscopy module in bench top settings has yielded preliminary results suggesting a linear response in the impedance range of interest (100- 700 kΩ) with a resolution for impedance changes in the sub-kΩ range. In-vitro and Early animal work has demonstrated some discrepancies from comparative data, and this troubleshooting this needs to be the next item on the research agenda. The data generated so far, however, appears promising that once the immediate issues are solved, impedance spectroscopy will be successfully implemented as part of a recording device, and data from this module will provide the first in depth look into the mechanism of signal variability and device failure in chronic implants.

The bipolar stimulation engine described in this work provides a unique opportunity for integrated patterned microstimulation for a closed-loop neural prostheses. Benchtop testing has validated system functionality and dynamic range. The DACs are however ~~highly~~ significantly non-linear and susceptible to some significant process variations, and need to be evaluated further to understand if they can be utilized in animal experiments when coupled with appropriate with charge-balance techniques.. Future work in this arena will focus both on utilization of this chip for animal experiments as well as an expanded 100-channel redesign with larger dynamic range (1 μA – 1mA) for a self-reliant charge-balanced stimulation system.

The horizons of the BCI field are constantly expanding. The overarching goal of this work was to provide additional access and information about the nature of the brain-implant interface through impedance spectroscopy and patterned cortical microstimulation. Development of these tools thus serves as the next set of tangible advances toward the ultimate goal of a smart, efficient implantable neural prosthetic sensor system.

6.4 References

1. Seo, Dongjin, Jose M. Carmena, Jan M. Rabaey, Elad Alon, and Michel M. Maharbiz. "Neural dust: An ultrasonic, low power solution for chronic brain-machine interfaces." arXiv preprint arXiv:1307.2196 (2013).

2. Negi, S., R. Bhandari, L. Rieth, and F. Solzbacher. "In vitro comparison of sputtered iridium oxide and platinum-coated neural implantable microelectrode arrays." Biomedical materials 5, no. 1 (2010): 015007.

3. Negi, Sandeep, Rajmohan Bhandari, and Florian Solzbacher. "Morphology and electrochemical properties of activated and sputtered iridium oxide films for functional electrostimulation." (2012).

4. Verma, Naveen, and Anantha P. Chandrakasan. "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes." Solid-State Circuits, IEEE Journal of 42, no. 6 (2007): 1196-1205.

5. Yeager, Doug, William Biederman, Nathan Narevsky, Jaclyn Leverett, Ryan Neely, Jose M. Carmena, Elad Alon, and Jan M. Rabaey. "A 4.78 mm 2 fully-integrated neuromodulation SoC combining 64 acquisition channels with digital compression and simultaneous dual stimulation." In VLSI Circuits Digest of Technical Papers, 2014 Symposium on, pp. 1-2. IEEE, 2014.

6. Harrison, Reid R., Paul T. Watkins, Ryan J. Kier, Robert O. Lovejoy, Daniel J. Black, Bradley Greger, and Florian Solzbacher. "A low-power integrated circuit for a wireless 100-electrode neural recording system." Solid-State Circuits, IEEE Journal of 42, no. 1 (2007): 123-133.

7. Shahrokhi, Farzaneh, Karim Abdelhalim, Demitre Serletis, Peter L. Carlen, and Roman Genov. "The 128-channel fully differential digital integrated

neural recording and stimulation interface." Biomedical Circuits and Systems, IEEE Transactions on 4, no. 3 (2010): 149-161.

8. Olsson, Roy H., Derek L. Buhl, Anton M. Sirota, Gyorgy Buzsaki, and Kensall D. Wise. "Band-tunable and multiplexed integrated circuits for simultaneous recording and stimulation with microelectrode arrays." Biomedical Engineering, IEEE Transactions on 52, no. 7 (2005): 1303-1311.

9. Blum, Richard A., James D. Ross, Edgar A. Brown, and Stephen P. DeWeerth. "An integrated system for simultaneous, multichannel neuronal stimulation and recording." Circuits and Systems I: Regular Papers, IEEE Transactions on 54, no. 12 (2007): 2608-2618.

10. Gryboś, Paweł, Piotr Kmon, Mirosław Żołądź, Robert Szczygieł, Maciej Kachel, Marian Lewandowski, and Tomasz Błasiak. "64 channel neural recording amplifier with tunable bandwidth in 180 nm CMOS technology." Metrology and Measurement Systems 18, no. 4 (2011): 631-644.

11. LTC 2366 datasheet. Accessed April 27th, 2016. http://www.linear.com/product/LTC2366.

12. Carlos Azeredo-Leme, Pedro Figueiredo, Manuel Mota. Scalable Architectures for Analog IP on Advanced Process Nodes. Accessed April 27th, 2016.

https://www.synopsys.com/Company/Publications/SynopsysInsight/Pages/Art5-data-converters-IssQ3-13.aspx?cmp=Insight-I3-2013-Art5

13. Arfin, Scott K., and Rahul Sarpeshkar. "An energy-efficient, adiabatic electrode stimulator with inductive energy recycling and feedback current regulation." Biomedical Circuits and Systems, IEEE Transactions on 6, no. 1 (2012): 1-14.

14. Lee, Hyung-Min, Ki Yong Kwon, Wen Li, and Maysam Ghovanloo. "A Power-Efficient Switched-Capacitor Stimulating System for Electrical/Optical Deep Brain Stimulation." Solid-State Circuits, IEEE Journal of 50, no. 1 (2015): 360-374.

15. Gibson, Sarah, et al. "An efficiency comparison of analog and digital spike detection." Neural Engineering, 2009. NER'09. 4th International IEEE/EMBS Conference on. IEEE, 2009.

16. Harrison, Reid R. "A low-power integrated circuit for adaptive detection of action potentials in noisy signals." In Engineering in Medicine and Biology Society, 2003. Proceedings of the 25th Annual International Conference of the IEEE, vol. 4, pp. 3325-3328. IEEE, 2003

17. Barati, Saied, and Amir M. Sodagar. "Adaptive spike detection method based on capacitor arrays dedicated to implantable neural recording microsystems." In Engineering in Medicine and Biology Society (EMBC), 2010 Annual International Conference of the IEEE, pp. 6445-6448. IEEE, 2010.

18. Gibson, Sarah, Rodney Chandler, Vaibhav Karkare, Dejan Marković, and Jack W. Judy. "An efficiency comparison of analog and digital spike detection." In Neural Engineering, 2009. NER'09. 4th International IEEE/EMBS Conference on, pp. 423-428. IEEE, 2009.

19. Gagnon-Turcotte, G., C-O. Dufresne Camaro, and B. Gosselin. "Comparison of low-power biopotential processors for on-the-fly spike detection." In Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, pp. 802-805. IEEE, 2015.

20. Li, Hongge, Huixin Bai, Qicheng Xu, and Tongsheng Xia. "Low-power MicroV rms noise neural spike detector for implantable interface microsystem device." Microelectronics Reliability 55, no. 5 (2015): 807-814.

21. Wu, Tong, Jian Xu, Yong Lian, Azam Khalili, Amir Rastegarnia, Cuntai Guan, and Zhi Yang. "A 16-Channel Nonparametric Spike Detection ASIC Based on EC-PC Decomposition." (2015).

22. Datta-Chaudhuri, Timir, Bathiya Senevirathna, Alexander Castro, Elisabeth Smela, and Pamela Abshire. "An active micro-electrode array with spike detection and asynchronous readout." In Biomedical Circuits and Systems Conference (BioCAS), 2014 IEEE, pp. 588-591. IEEE, 2014.

23. Kmon, Piotr. "NRSD8-Neural recording and spike detection multichannel integrated circuit designed in 180nm CMOS technology." In Mixed Design of

Integrated Circuits and Systems (MIXDES), 2013 Proceedings of the 20th International Conference, pp. 255-258. IEEE, 2013.

24. Zeinolabedin, Seyed Mohammad Ali, Anh Tuan Do, Kiat Seng Yeo, and Tony Tae-Hyoung Kim. "Design of a hybrid neural spike detection algorithm for implantable integrated brain circuits." In Circuits and Systems (ISCAS), 2015 IEEE International Symposium on, pp. 794-797. IEEE, 2015.

25. Yang, Yuning, C. Sam Boling, Awais M. Kamboh, and Andrew J. Mason. "Adaptive Threshold Neural Spike Detector Using Stationary Wavelet Transform in CMOS." Neural Systems and Rehabilitation Engineering, IEEE Transactions on 23, no. 6 (2015): 946-955.

26. Eftekhar, Amir, Sivylla E. Paraskevopoulou, and Timothy G. Constandinou. "Towards a next generation neural interface: Optimizing power, bandwidth and data quality." In Biomedical Circuits and Systems Conference (BioCAS), 2010 IEEE, pp. 122-125. IEEE, 2010.

Appendix I

Design for Translation

The field of Neural Prosthetics is a vibrant and dynamic one. Several groups are developing cutting edge technologies, yet the commercial space for implantable systems is not expanding at a commensurate pace. There are numerous challenges to translation of an academic endeavor, and the need for extensive testing and documentation to meet biomedical regulatory requirements is at the forefront of the list. The fully implantable, hermetically-sealed, wireless recording system described in Chapter 2 is currently on the pathway for translation to a human-grade device for clinical trials (referred to as NeuroComm in this Appendix). A significant amount of effort was expended in the first phase of the translation activity to bring the ASIC documentation up to regulatory standards. The purpose of this document is to serve as an overview of appropriate documentation approaches during ASIC development, geared toward minimizing the overhead associated with the translation process.

The list of documentation described in this appendix was generated in collaboration with a CSEM (Swiss Center for Electronics and Microtechnology). They served as a 3rd party reviewer, and guided the filling of gaps in ASIC documentation andtest data. This process, termed the “ASIC Gap Analysis” here, was undertaken with the goal to yield full data sheets for each of the ASICs in the NeuroComm device.

ASIC Documentation

There are three key constituents of a comprehensive engineering documentation repository for an ASIC, as outlined below:

i. **System Requirements Document:** This document describes the basic engineering specifications for the overall system that the ASIC is part of. It is the first piece of documentation to be created (prior to design initiation). This includes derivations of all values used as upper and lower bounds of design parameters. For the NeuroComm system, there is a single system requirements document, which covers the specs pertaining to the Amplifier, Controller and Transmitter ASICs, and is included as Appendix I-A.

ii. **Design File Directories:** A full list of documents to be included in the design directory is shown in Table A1.1. A design directory for each ASIC should be created at the time of initial design. The design database is the most extensive constituent of the design directory. It is important to save design files and standard cell libraries from Cadence (or alternative ASIC-design software) such that a 3rd party reviewer may be able to easily import the design into their computer for review. It is good practice to save all simulation test platforms as well, so simulation data may readily be re-generated for verification. Furthermore, it is crucial to save a copy of the design schematics in a multi-platform file format such as pdf (for access by reviewers who may not have the appropriate ASIC design-software package).

ASIC design description	
Circuit description	Describes basic functionality of ASIC (This should agree with the System Requirements document).
Block diagram	Top-level diagram with main sub blocks
I/O description	ASIC pinout with description of each pin
Bonding diagram	Includes Package description
Electrical specifications	Electrical parameters and performance (derived from simulation and testing): All data should be saved in report format - *Simulations*: Transient, AC, noise (when appropriate), process corners - bench top testing results
Digital Interface	
Control interface description	Description how to access chip's registers, if any
Control register description	Description of control and status registers, if any
Application diagram	Shows ASIC in application context - If there is more than one ASIC, an interface communication protocol and timing diagram should be furnished
Test specification	Specifies ASIC production tests - List of benchtop tests to validate that the fabricated ASIC functions as described by the documents above
Design data base	
All	
Block specifications	Functional description and specifications of each block
Schematics	Transistor level schematics (hierarchical to top level)
Block design reports	Simulation results on block level (optional).
ASIC design report	Short design description and simulation results
Design review results	Meeting minutes or filled in checklist form
Digital Blocks	
RTL code	Verilog / VHDL sources of digital block(s)
Gate level netlist	Netlist resulting from place & route
STA timing report	Results of static timing analysis
Formal verification report	Results of RTL vs netlist check
Test patterns	only if scan test implemented
Layout	

DRC/LVS/ERC/Antenna report	Check of design rules and layout vs schematic
Characterization	
Test board schematics	PCB board layout/schematics for system-level testing
Verification plan	Listing of test-points and associated tests conducted on the system to verify performance
ASIC characterization report	Report from characterization tests conducted (as described by the documents in this section)
Latch up/ESD report	ESD and Latch-up testing on fabricated devices

Table A1.1: Constituents of Document Repository

Figure A1.1 shows one approach to organizing the information for a given ASIC (the amplifier ASIC in this particular case). The block diagram, pinout, design database and communication protocols are all available pre-fabrication, whereas electrical specifications and characterization require pre-and-post fabrication data.

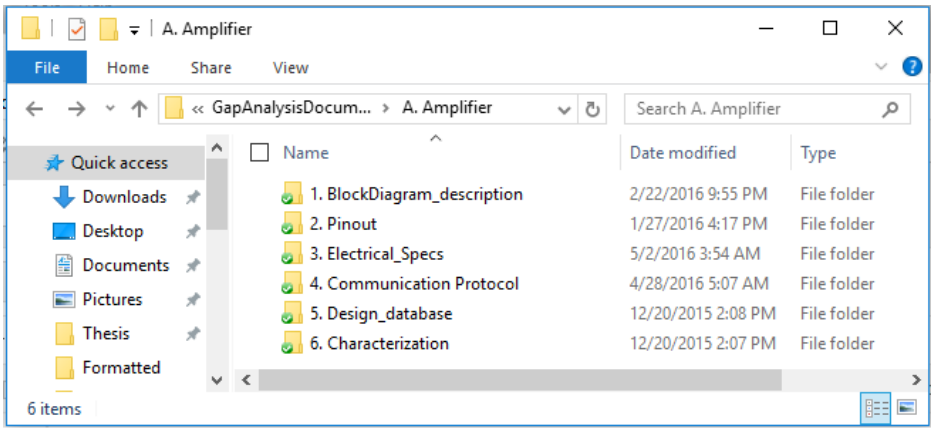


Figure A1.1: Design File Repository Organization

iii. **ASIC Data sheet**: Once pre-and-post fabrication testing is completed, a full data sheet should be generated for each ASIC incorporating simulation and test data. Appendix I-B demonstrates a copy of the

Amplifier ASIC data sheet, as generated from the ASIC documentation in Figure A1.1.

Risk Analysis

The data sheets generated in (iii) above are then used for the final step of the ASIC Gap Analysis. This is to conduct a risk analysis of the system identifying the device's failure mechanisms as well as approaches to mitigate the impact of those failures on device performance and safety. The risk analysis of the NeuroComm device is provided as an example in Appendix I-C.

The approach to documentation outlined in this Appendix is modeled after the process followed in commercial ASIC-design houses. For the NeuroComm device, we had to conduct a retrospective analysis to generate many of the above-mentioned items. This endeavor took several months, thus impacting overall project timelines. Furthermore, some items, such as STA timing reports could not be generated retrospectively. That data was thus lost, and associated risks could not be mitigated. Pursuing a well-organized documentation approach from the get-go would not ensure timely completion of translational goals, but would allow for design reuse in the context of a different application.

Appendix I-A

NeuroComm System Requirements Document

System Objectives:

1. Capture broadband Neural data (100 mHz – 5-7 kHz) through an array of 100 micro-machined silicon-based microelectrodes with electrode impedances in 100-500 kΩ range ("Utah array").

2. Analog to Digital conversion of multichannel neural data using commercially available ADCs (off-chip, but part of overall system).

3. Encryption of digital data for data security.

4. Transmission of encrypted data with adequate output power for a receiver ~ 1 m away.

5. Minimize system power consumption to limit ambient temperature increase <2°C and to maximize time between battery recharges to >4 hours

6. Minimize transistor level electronic noise for improved signal-to-noise ratio in recordings.

Requirements for the Amplifier ASIC:

1. **Preamplifiers:** The considerations in preamplifier design are as follows:

a. Amplitude and Frequency:

Neural data spans a frequency range from a few Hz- 5 kHz. Signal sources contributing to data are broadly classified in 2 classes:

i. *Single and Multiunit activity (SUA/MUA)* at the level of individual neural cell action potentials (100μV- 1mV at 300Hz- 5kHz)

ii. *Local Field potentials (LFPs)* or cumulative electrical activity from larger populations of neurons (50μV- 1mV at 10Hz- 300Hz)

Thus, the **amplitude ranges of detection are ~50μV- 1mV**. Frequencies of interest are **10 Hz- 5kHz.** Collectively, measurement of these are referred to as "extracellular neural recordings".

b. Signal to Noise Ratio and total System Noise:

The Amplifier ASIC must be able to record the signals described above with a signal to noise ratio of at least 3. Given that ~50 μV is the smallest voltage of interest, total electronic system noise must be < ~15 μV. The two largest sources of noise in the system are:

i. *Johnson noise in the neural electrodes* (impedances 100-500 kΩ) and df =5kHz

$$Vn^2 = 4kTRdf$$

For the Utah array, Vn_{RMS}=

$$\sqrt{4 * 1.38 * 10^{-23} * 300 * (100 - 500) * 10^3 * 5 * 10^3}$$

$$= 2.8 \text{ -}6.4\ \mu V_{RMS}$$

ii. *CMOS transistor noise:* There are several sources of transistor noise, and the predominant ones to be considered are shot and flicker (1/f) noise. These have to be minimized so electronic noise from transistors is less than or equal to Johnson noise contribution from (i) above.

c. DC rejection:

There are large DC offsets due in extracellular recordings due to the electrochemical interface between neural tissue and metallic electrodes. Neural signal amplifiers must reject the DC offset while preserving capability to record the very low frequencies that are part of LFP with adequate SNR. The amplifier design, therefore, needs to implement a high-pass filter with a 3dB cut-off frequency <10 Hz, best achieved by a "MOFET pseudo-resistor" feedback structure.

2. Analog to Digital Conversion:

Conversion of the analog signal recorded by the preamplifiers must be achieved by a synchronized multiplexing by amplifier ASIC and sampling by the off-chip ADC,

under the command of the controller ASIC. Sampling rates per channel must satisfy the Nyquist criteria:

$f_{sample} > 2 * f_{max}$ where f_{max} is the maximum recorded frequency of interest.

For neural data, f_{max} is ~ 7 kHz, sampling rate must thus be >15 kHz per channel.

a. Multiplexing:

The system is implemented using commercial 12-bit ADCs for digitization of signals from a 100-channel system. This translates into one ADC per 50 channels. The amplifier ASIC must have:

i. the ability to individually address each of the 100 channels

ii. provide a low output impedance pathway for sampling by ADC (Buffer amplifier)

iii. Enable power savings by allowing maximal number of amplifier to be in "standby mode" when their output is not being actively digitized

Requirements for the Controller Chip

The Controller chip must function as the command center for the implantable system. The following lists the tasks to be managed by the Controller chip:

1. System clock generation/recovery:

The implantable system may receive RF power/clock or both. In either case, the Controller Chip must have a mechanism to recover a clock for use on-board the implant, both within the controller chip itself as well as the Amplifier chip (for multiplexing) and the ADCs (for sampling).

2. Interface management for Analog to Digital Conversion and Data Transmission:

The Controller Chip must interface with the off-chip ADCs and the amplifier chip to enable coordinated multiplexing, sampling and digitization. It must then capture the digitized stream and interface with the transmitter chip for transmission of digitized data.

a. Amplifier Chip:

i. The Controller must set the frequency for multiplexing operations.

ii. The Controller must receive any end-of-frame signal from the amplifier and reflect his in the transmitted data to facilitate appropriate data decoding (SYNCH word generation).

b. Analog to Digital Converters:

i. The Controller Chip must issue a clock signal for sampling, synchronized with multiplexing signal from the amplifier ASIC.

With a sampling rate of >15 kSamples/second/channel and 50 channels/ADC in a 100-channel system, a 12-bit ADC must operate at >750 kSamples/second

ii. In order for low-power operation, the Controller chip should manage enable/disable functionality of the ADCs to minimize power consumption when not in use.

c. Transmitter Chip:

i. The Controller chip must provide a digitized data stream for transmission.

3. Data Encoding for transmission:

Data must be encoded for wireless transmission using an encoding scheme that allows for data recover without clock. The Controller Chip must coordinate G. E. Thomas Manchester Encoding for this purpose.

Requirements for Transmitter Chip

The Transmitter Chip must be able to receive the Manchester-encoded data from the controller chip, and transmit is wirelessly to a receiver a short distance away. In this current system, the transmitter chip only needs to have 1 dedicated channel for neural data output.

1. Data Rate:

The datastream from the controller chip is composed of 100-channels of sequential amplifier data at 20 ksamples/second (with possible increase to 30 ksamples/second)

and 12-bits/sample (with possibility of expansion to 16 bits/channel). This sets a minimum transmission data rate requirement of 48 MBps . The initial transmitter design should have a data rate of at 48MBps, and ideally have data rate > 100MBps.

2. Transmission Frequency:

The transmitter should be designed for operation in short-range communication frequency band (few GigaHertz). Additionally, the frequency range should be an FCC non-medical band to prevent issues of interference with other biomedical devices/security. Given these considerations, 2.9 – 3.8 GHz frequency range is selected as appropriate for this application.

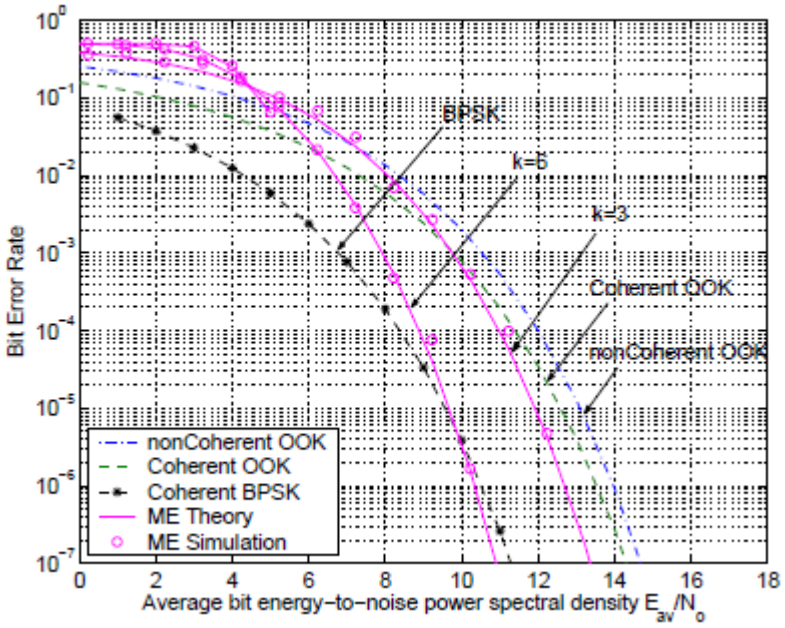
3. Transmission distance:

The wireless system is designed to enable free movement of the subject. The transmitter must thus be able to work with an omnidirectional remote receiver antenna. This design for high-data-rate short range communication should have adequate output power for a receiver at least 1 m away, and ideally 2-3 meters away.

4. Power consumption and output power optimization:

The transmitter chip design must optimize for low-power consumption and efficiency to allow for longer battery life between recharges. These specifications are best met by using phase-shift keying approaches such as BPSK or OOK. The transmitter design should this employ this approach. Figure 1 demonstrates the relationship between bit-error-rate and signal-to-noise ratios for various modulation schemes.

Based on this figure, SNR for an OOK-approach to work reliably requires SNR > 12.5 dB.



The overall power consumption for the transmitter must be minimized to extend battery life and minimize local heat dissipation. In accordance with FDA regulations for class 3 devices, power consumption for a safe implant must cause <2°C increase in local temperature. As such, the transmitter must be designed to have <10 mW total power dissipation.

Appendix I-B

BigPearl Amplifier ASIC Datasheet

1. Table of Contents

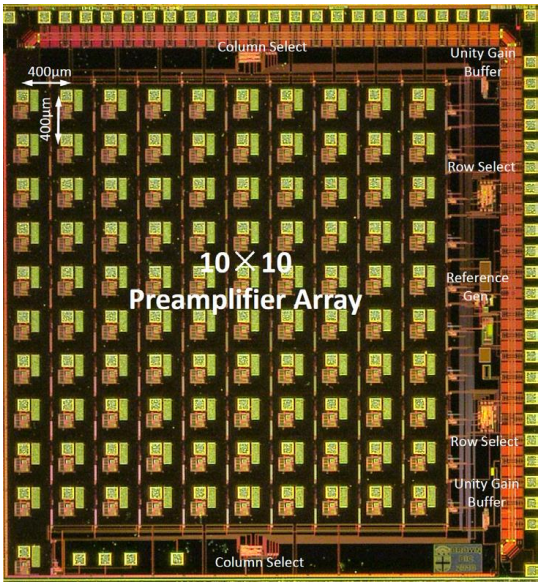


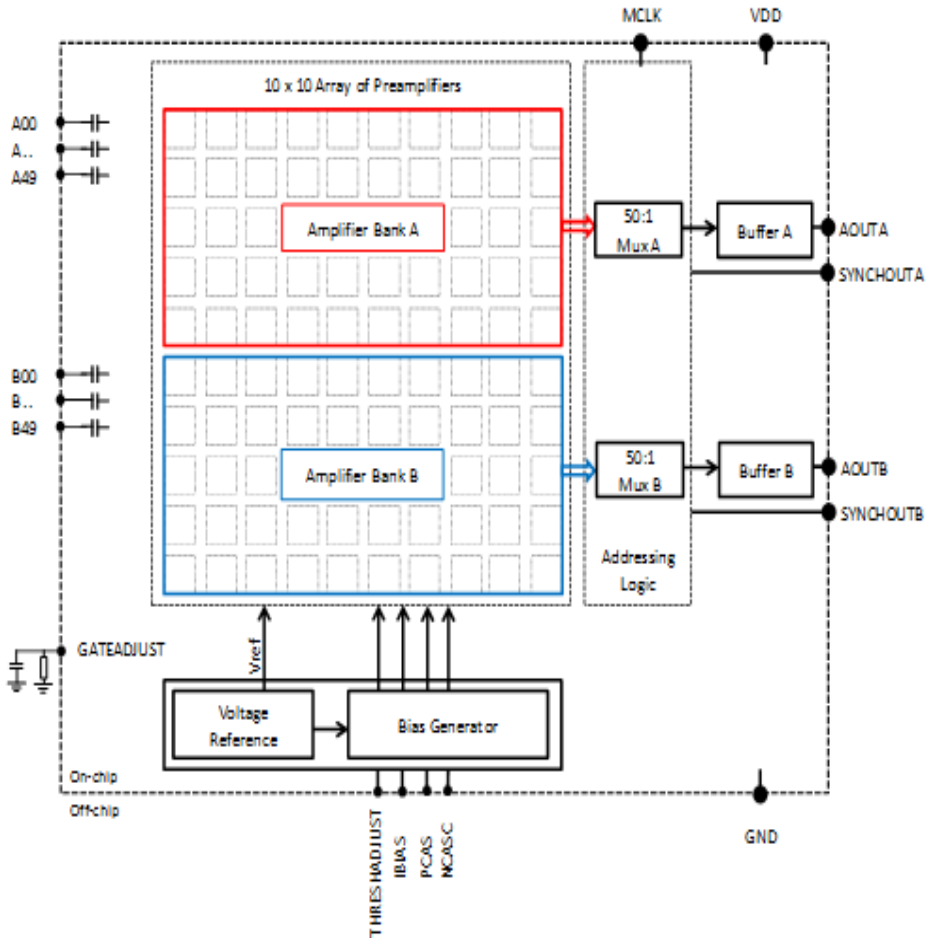
Figure 1 Microphotograph of the 100-ch preamplifier ASIC

2. Chip Description

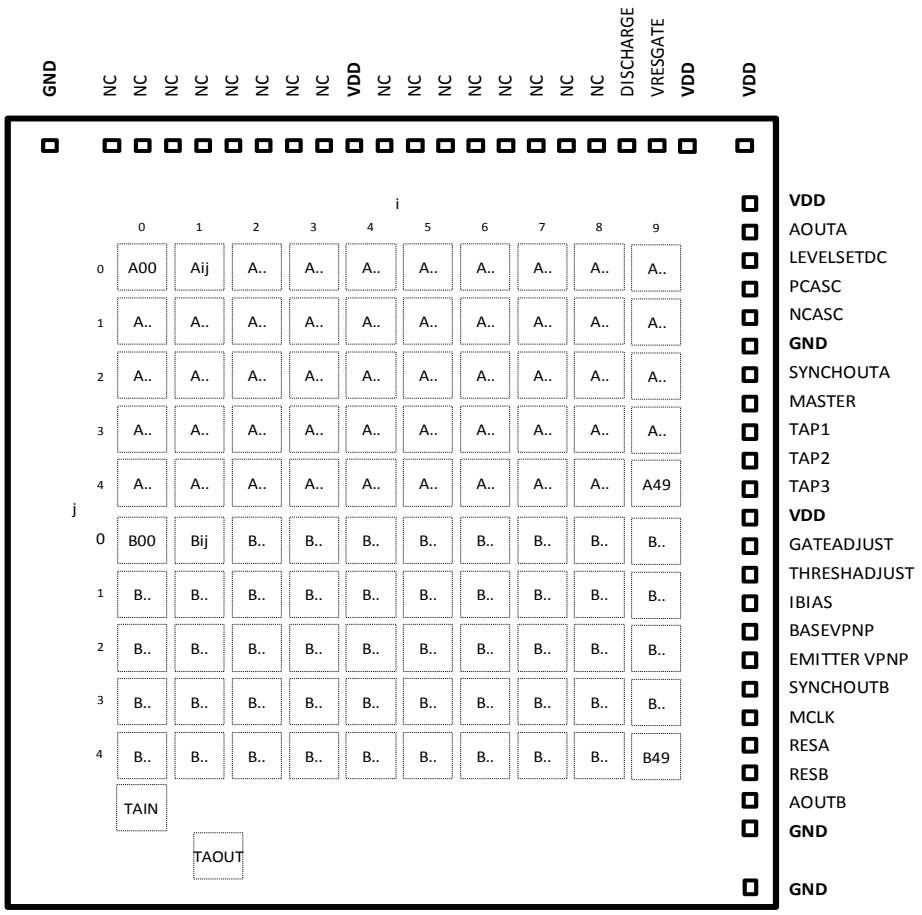
BigPearl is a custom Application Specific Integrated Circuit with 100 parallel broadband neural recording channels of preamplifiers arranged in a 10 by 10 array and two fifty channel analog multiplexers.

The incoming neural signal on each channel is conditioned and amplified by a low-noise low-power preamplifier implemented in the ASIC. The preamplifier uses a capacitive-feedback, folded cascade Operational Transconductance Amplifier configuration with a source follower output buffer. The closed-loop gain of the OTA is 46dB and the bandwidth is 1 mHz(tunable)-7.8kHz.

A 10pF internal capacitor completely rejects any DC offset voltage at the input electrode, eliminating problems with built-in potential at electrode-tissue interface.



3. I/O Description



3.2 Pin description

Pin	Type	Function
A00-A49	Analog inputs	Amplifier input pads for Bank A.
B00-B49	Analog inputs	Amplifier input pads for Bank B.
VDD		Power Supply for chip.
GND		Ground. Connect to reference electrode.
AOUTA	Analog output	Multiplexed analog output for Bank A amplifiers.
AOUTB	Analog output	Multiplexed analog output for Bank B amplifiers.
LEVELSETDC		Not connected.
PCASC	Output	Test pad for bias circuitry PMOS cascode voltage.
NCASC	Output	Test pad for bias circuitry NMOS cascode

Figure 3 Pin Designation

SYNCHOUTA	Output	Signal completion of one cycle of sampling (50 amplifiers for Bank A).
SYNCHOUTB	Output	Signal completion of one cycle of sampling (50 amplifiers for Bank B).
MASTER	Input	Master/Slave configuration signal. Respectively hard-wired high or low. In Master mode, internal sampling clock is phase-shifted by 180° for bank B. In Slave configuration, clock is shifted for bank A.
TAP1-3	Output	Test pads for bias source resistor voltage.
GATEADJUST	Analog	Tunes high-pass filter frequency.
THRESHADJUST		Tunes bias current for appropriate amplifier gain.
IBIAS	Output	Test pad for bias current.
BASEVPNP		Not connected.

EMITTERVPNP		Not connected.
MCLK	Input	Master clock input for multiplexing. When MASTER is high, Bank A is incremented on a rising edge, Bank B is incremented on a falling edge.
RESA/RESB		Not connected.
TAIN	Analog input	Test amplifier input. Connect to ground if this function is not used.
TAOUT	Analog output	Test amplifier output. Do not connect if unused.
DISCHARGE		Connect to ground.
VRESGATE		Do not connect.

Table 1 Pin Description

4. Electrical Characteristics

4.1 Typical Values

T_A = 27°C, VDD = 3V unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Comments
V_{DD}	Supply voltage		2.8	3.3	3.6	V	A 0.1µF power supply bypass capacitor should be used.
A_M	Amplifier differential gain	Mid-band gain between f_L and f_H		199.9 46		V/V dB	
f_L	Amplifier low-frequency 3dB cut-off frequency	Set by off-chip RC	0.001		100	Hz	1-pole roll-off below f_L
f_H	Amplifier high-frequency 3dB cut-off frequency			7.8		kHz	1-pole roll-off above f_H
f_{MCLK}	Sampling clock			1		MHz	
V_{AMP-AC}	Amplifier input voltage range		-2		2	mV	
V_{AMP-DC}	Amplifier voltage allowable DC offset		-0.7		0.7	V	ESD diodes conduct to ground as DC offset increases
CMRR	Amplifier Common Mode Rejection Ratio		60			dB	
PSRR	Amplifier Power Supply Rejection Ratio		50			dB	
C_{IN}	Amplifier input capacitance			10		pF	
|Zin|	Amplifier input Impedance	f_L = 1Hz		16		GΩ	Depends on high-pass cut-off frequency
V_{NOISE}	Amplifier input-referred noise	1Hz to 10kHz		2.83		μV_{rms}	Varies slightly with amplifier bandwidth

Table 2 Typical values

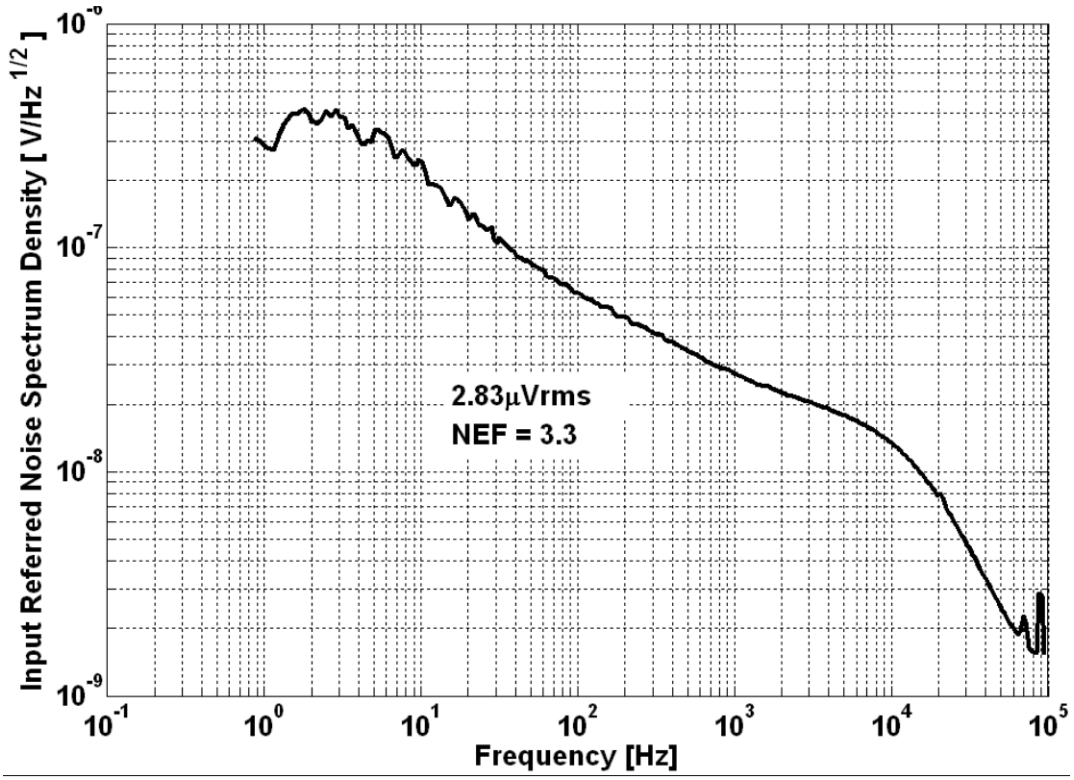


Figure 4 Noise spectrum density

The noise spectrum density of the preamplifier shows an input referred noise of 2.83μV_{RMS} over a frequency range of 1 Hz to 10 kHz and a Noise Efficiency Factor of 3.3.

4.2 Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply voltage	-0.3	5.5	V
Analog Inputs DC	-0.7	0.7	V
Digital Inputs	-0.3	5.5	V
Digital Outputs	-0.3	5.5	V
Electrostatic Discharge (Analog Inputs)		2.0	kV

Table 3 Absolute Maximum Ratings

4.3 Electrostatic Discharge

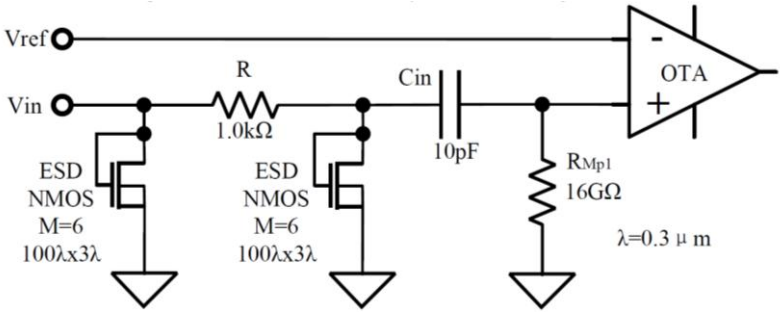


Figure 5 ESD protection circuits for the preamplifier input on the preamplifier ASIC

The ESD human-body model used for testing this device followed the internationally widely use JEDEC standard: JESD22-A114D. The circuit uses two large NMOS transistors each consisting of six parallel devices having width to length ratios of 30 × 0.9μm as the voltage limiting and energy absorbing elements. The gate and drain of each transistor are connected together to the signal line while the source and substrate connections are tied to ground. The two transistors form a pi-network between the input pad and the input to the preamplifier. A 1kΩ resistor, the third element of the pi-network, connects the two transistors. For a positive overvoltage input, the transistors act as diode-connected MOSFETs, turning on at the threshold voltage of

0.7V. For a negative input, the drain to substrate junction is forward biased and the local substrate connections assure a low forward voltage even at high current. This design guarantees that even if the surge voltage seen by the first stage NMOS exceeds the break down voltage of the input capacitor and input PMOS gate oxide, the voltage applied to those elements will not. One advantage of this protection circuit is that it does not provide any path from the I/O pad to the supply voltage even after failure of either junctions or gate oxide.

5. Timing Diagram

The entire 100 preamplifiers are divided into two groups of 50 preamplifiers each. The outputs from the preamplifiers in each group are multiplexed onto one of two analog outputs (AOUT_A and AOUT_B). This is run at a 1MHz clock. The clock is 180° phase shifted for B bank when MASTER input pad is wired to V_{DD}, and 180° phase shifted for A bank when it is wired to GND. The two multiplexed analog neural signals are buffered with unity gain buffers. When an entire cycle of sampling is complete, the corresponding SYNCHOUT_x signal is asserted by the amplifier. This signal allows the controller to delay the next sampling cycle by holding the clock. At this time, the AOUT_x signal is still putting out the valid voltage of the last channel.

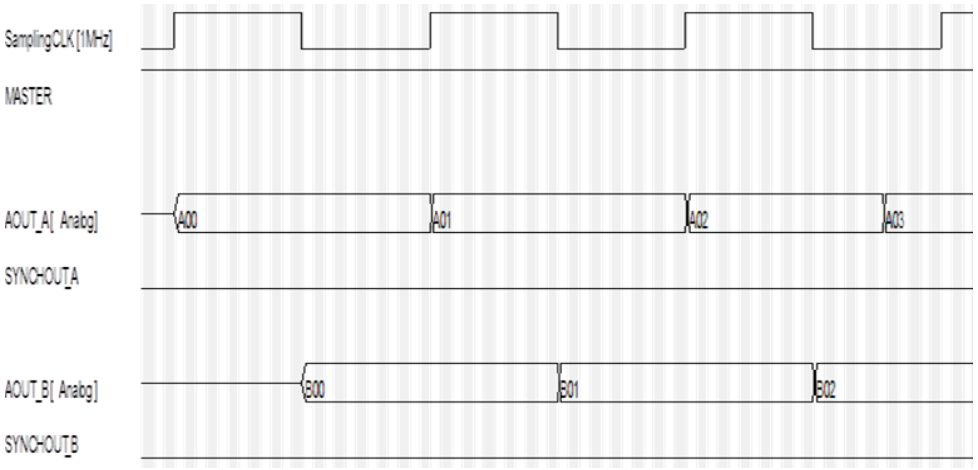


Figure 6 Timing Diagram - First channels

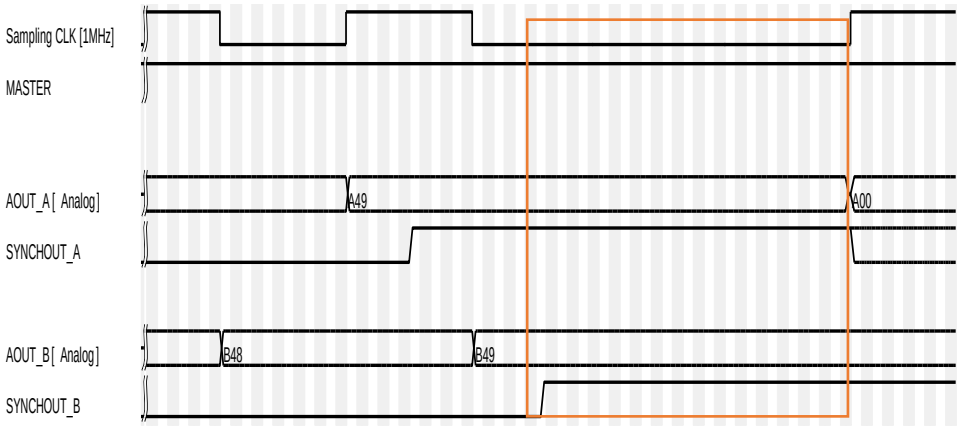
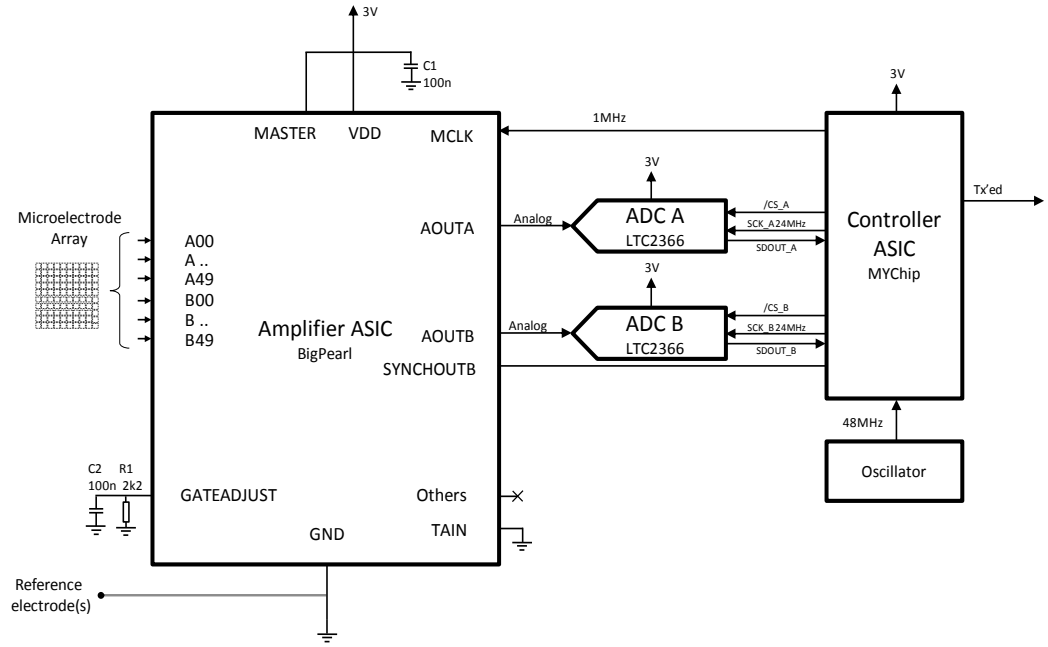


Figure 7 Timing Diagram - Last channels

With a 1MHz main clock, an entire cycle of sampling is completed in 50µs which leads to a maximum sampling rate of 20 kSps/ch.

6. Typical Application



	RES SMD 2.2K OHM 1%			
R1	1/10W 0402	0402	2.2kΩ	ERJ-2RKF2201X

Table 4 Bill of Materials

The Amplifier ASIC relies on the controller ASIC to provide a sampling clock signal which is used as the switching clock for sampling from individual amplifiers by MUX A and B. The digital controller provides a Chip Select signal (/CS_A and /CS_B) to each ADC respectively to initiate the 14-cycle conversion cycle for ADC. There is a 2 cycle "enable" overlap between the 2 ADCs to enable consecutive read out from each ADC. When one entire cycle of sampling is complete (50 channels on MUX A and 50 channels on MUX B), the SYNCHOUTB signal is asserted by the amplifier chip, which triggers the insertion of a synch word into the output data stream by the digital controller. The Controller ASIC holds the sampling clock during this 1μs operation which leads to a sampling rate of 19.6 kSps/ch.

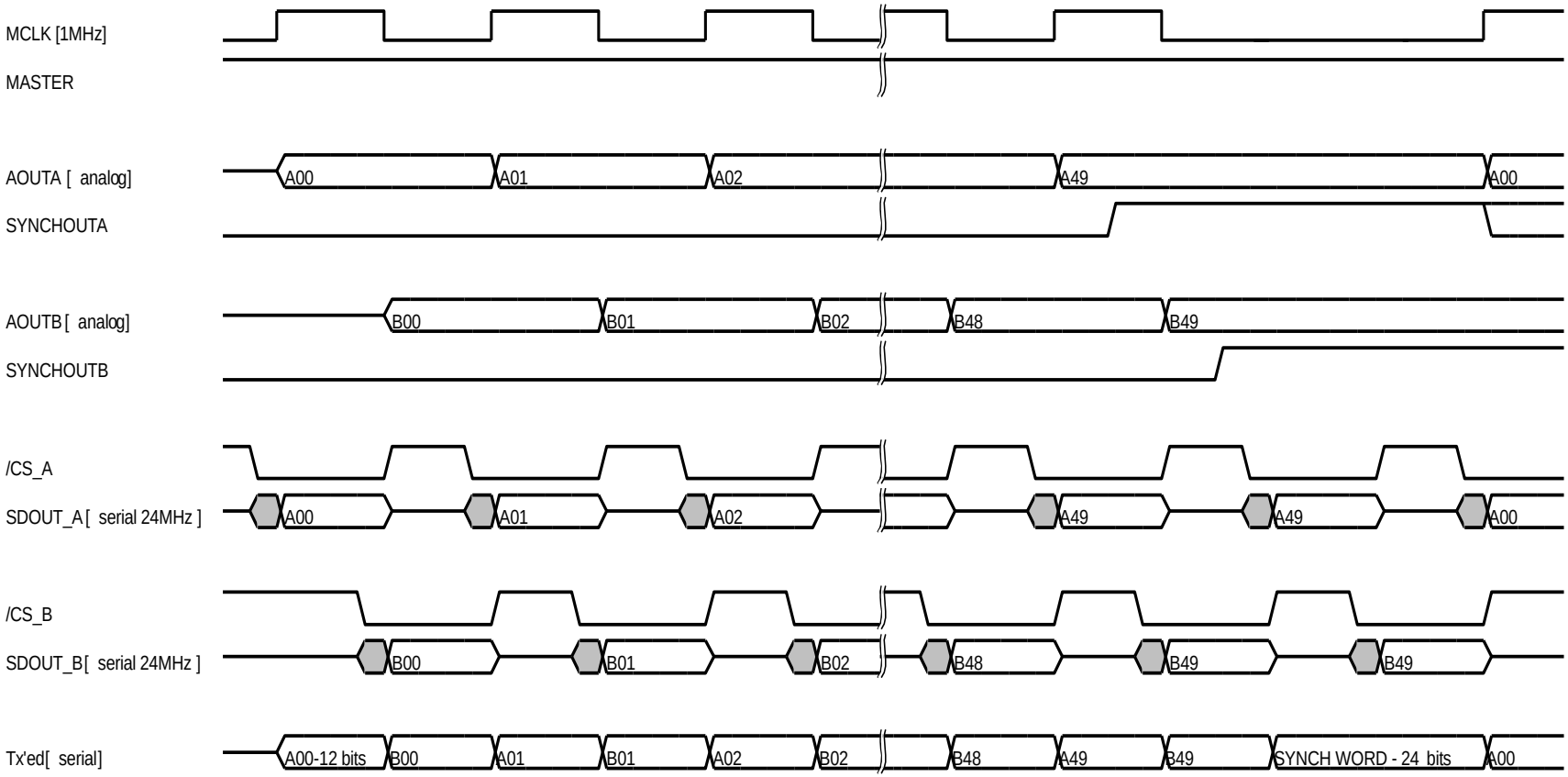


Figure 9 Timing diagram of a neural interface application

7. Footprint dimensions

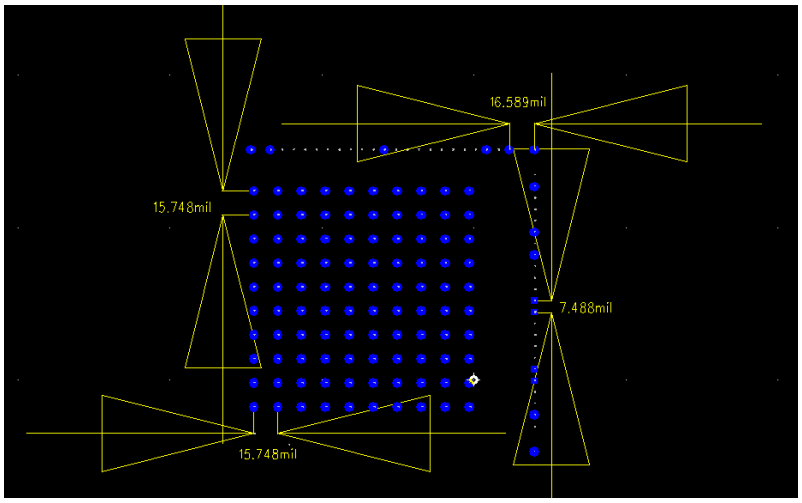


Figure 10 Footprint dimensions (mil)

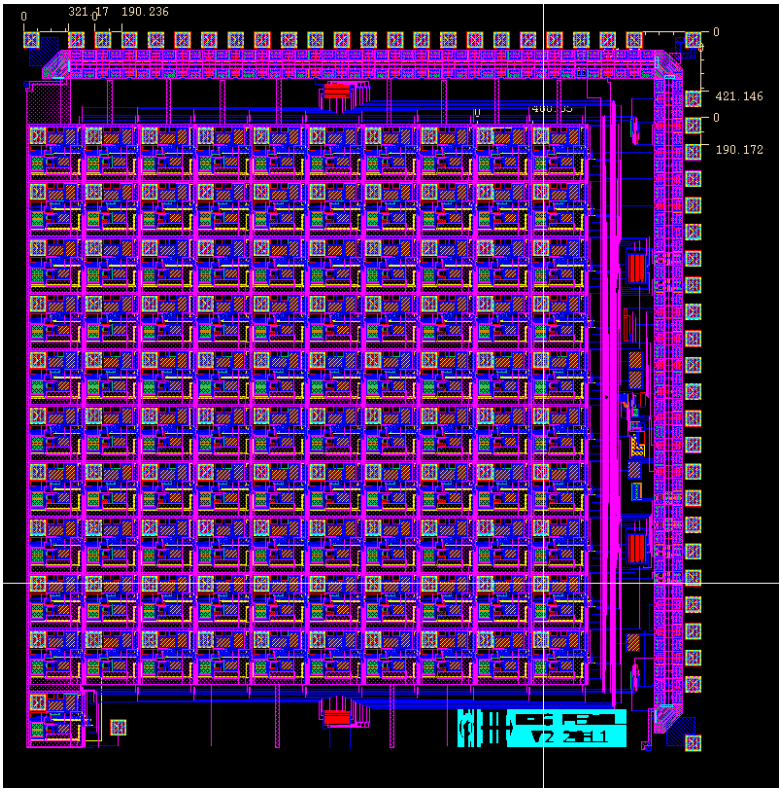


Figure 11 Chip dimensions (µm)

Appendix I-C

NeuroComm Risk Analysis Matrix

ID#	Name of Part / Component /	Cause / Sequence of Events	Hazardous situations	Harm	Initial risk*				Risk control / mitigation measure	Residual risk*			
		What leads to the hazardous situation / Under which circumstances?	What is the resulting hazardous situation?	What may happen to others / environment?	Severity *	Probability *	Detectability *	RPN *	Risk control / mitigation measure description	Severity *	Probability *	Detectability *	RPN *
RA-D001	Amplifier Chip	Output saturates	Input referred offset too large	Chip not usable	10	5	4	200	Simulate offset (Monte Carlo), make transistors of the amplifier's differential pair large enough	10	2	1	20
RA-D002	Amplifier Chip	Output too noisy	Input referred noise too large	Performance degradation	8	6	3	144	Make noise simulation of the readout	8	2	3	48
RA-D003	Amplifier Chip	Output too noisy	Cross talk between channels	Performance degradation	8	6	8	384	Make simulation on extracted layout	8	2	3	48
RA-D004	Amplifier Chip	Electrode inputs get damaged when connecting to brain	Electrostatic discharge	Chip not usable	10	3	5	150	Carefully review all I/Os (ESD protection) Make ESD tests on chip samples	10	3	1	30
RA-D005	Amplifier Chip	Charge injected into electrode-electrolyte interface	Charge density too large	Patient will be harmed	10	3	4	120	Calculate expected maximum charge injection	10	2	4	80
RA-D006	Controller Chip	Improper data acquisition	Problems interfacing the ADCs	Chip not functional	10	4	7	280	Map design on FPGA, verify together with ADC	10	2	1	20
RA-D007	RF Chip		RF power too high	Patient will be harmed				0					0
RA-D008	Amp+Ctrl+RF	Module gets too hot	Power dissipation too high	Patient will be harmed	9	5	7	315	Carefully estimate power consumption, verify on samples	9	2	1	18

Appendix II

This appendix demonstrates the parameters and analysis for technology scaling of the amplifier ASIC

ScalingPearl 5/15/2016 at 11:52 PM

Pearl scaling spreadsheet: 0.5 micron process sizes derived from the MM9/Pearl chip

Pearl Section				Pearl (um)		Scaled (um)		Scaled (λ)		MOSFET Bias and SS Parameters							
Pearl RefDes	# in par.	Type	Function	L	W	L	W	L	W	ID (ua)	gm	gds	Vov	VGS	VTH	Test VDS	Cas-code FOM
Preamplifiers:																	
M1/2	4	PMOS	input pair - note Pearl has 1.09 ua ID but new one will have 1.25 ua per.	10.8	56	10.8	51	36	170	1.25	1.66E-05	2.06E-08	0.112	1.05	0.924	0.4	
M3	8	PMOS	tail bias sources - Pearl only has 7X	3.2	9.6	2.4	2.1	8	7	1.25	6.85E-06	2.33E-07	0.34	1.31	0.97	0.4	
M4	1	PMOS	cascode on current source	2.4	60	1.8	12.9	6	43	10	6.78E-05	9.44E-07	0.281	1.212	0.931	0.55	76
M4 Alt	8	PMOS	cascode on current source	2.4	n.a.	1.8	2.1	6	7	1.25	8.18E-06	1.06E-07	0.281	1.367	1.086	0.6	84
M7	2	PMOS	Mirror control	11.2	12.8	11.2	8.1	37	27	1.25	6.97E-06	1.57E-07	0.334	1.265	0.932	0.4	71.3
M8	2	PMOS	Mirror cascode	3.2	12.8	2.4	4.5	8	15	1.25	1.15E-05	5.79E-08	0.199	1.14	0.944	0.8	219
M11	4	PMOS	Follower PMOS (use 2 in scaled)	2.4	11.8	0.9	6.6	3	22	5	5.33E-05	5.34E-07	0.175	1.104	0.93	1.7	100
M12	1	PMOS	Follower current cascode	1.6	20.8	0.9	7.8	3	26	10	6.34E-05	1.69E-06	0.233	1.269	1.036	0.5	41.5
M13	1	PMOS	Follower current control	1.6	20.8	1.2	7.8	4	26	10	6.49E-05	9.71E-07	0.288	1.223	0.934	0.4	70
			pull-down currents - Pearl only has 4 of														
M5/6	5	NMOS	1.41 ua	24	14.4	24	6.9	80	23	1.25	8.48E-06	5.51E-08	0.33	1.052	0.712	0.45	
M9	2	NMOS	Cascode folding	3.2	4.8	2.4	3	8	10	1.25	1.68E-05	5.85E-08	0.176	1.123	0.946	0.8	329
M10	1	NMOS	Follower NMOS	2.4	4.8	1.2	2.4	4	8	1.25	1.55E-05	2.88E-08	0.191	1.27	1.078	2	525
M14	1	NMOS	Switch	1.6	11.2	0.6	4.5	2	15	RSW = 2.5K max							
M15	1	PMOS	Switch	1.6	22.4	0.6	10.5	2	35								
								0	0								
M16	4	PMOS	Base unit input and feedback resistors	4.8	4.8	2.4	2.4	8	8	0	TBD						

Pearl scaling spreadsheet: 0.5 micron process sizes derived from the MM9/Pearl chip

Pearl Section				Pearl (um)		Scaled (um)		Scaled (λ)		MOSFET Bias and SS Parameters							
Pearl RefDes	# in par.	Type	Function	L	W	L	W	L	W	ID (ua)	gm	gds	Vov	VGS	VTH	Test VDS	Cas-code FOM
								0	0								
Row Drivers								0	0								
M1	2	NMOS	Master current duplicate control	9.6	12.8	4.8	3	16	10	1.25	1.21E-05	7.97E-08	0.251	1.03	0.782	0.45	
M2	5	NMOS	NMOS cascode small	3.2	4.8	2.4	3	8	10	1.25	1.68E-05	5.85E-08	0.176	1.123	0.946	0.8	329
M3	1	NMOS	NMOS bias control	24	12.8	24	6.9	80	23	1.25	8.48E-06	5.51E-08	0.33	1.052	0.712	0.45	
M4	1	NMOS	NMOS cascode large	3.2	16	2.4	3	8	10	1.25	1.56E-05	5.34E-07	0.215	0.733	0.519	0.8	310
	5	NMOS	M4 alt. Small cascode			2.4	3	8	10	1.25	1.68E-05	5.85E-08	0.176	1.123	0.946	0.8	329
M5	5	NMOS	Current on/off switch	1.6	4.8	0.6	3	2	10	1.25							
M6	7	NMOS	Row current control	4.8	4.8	4.2	3	14	10	1.25	1.32E-05	8.78E-08	0.249	1.036	0.787	0.45	
								0	0								
M7	3	PMOS	Master current duplicate control - P side	3.2	9.6	2.4	2.1	8	7	1.25	6.85E-06	2.33E-07	0.34	1.31	0.97	0.4	
M8	3	PMOS	Master cascode	2.4	9.6	1.8	2.1	6	7	1.25	8.37E-06	4.98E-08	0.274	1.36	1.086	1.39	175
M9	1	PMOS	Row control	2.4	17.6	1.2	6.3	4	21	7.5	5.03E-05	7.26E-07	0.28	1.218	0.937	0.8	
M10	1	PMOS	Row cascode	1.6	17.6	0.9	6.3	3	21	7.5	5.76E-05	1.04E-06	0.235	1.273	1.038	0.8	59
M11	1	PMOS	Inverter top	2.4	8	0.9	3	3	10	n,a.							
M12	1	NMOS	Inverter bottom	2.4	4.8	0.9	1.5	3	5	n.a.							
Master Bias Generator																	
M1	11	PMOS	Base control transistor	3.2	9.6	2.1	2.1	7	7	1.25	7.43E-06	2.09E-07	0.314	1.285	0.971	0.4	
M2	16	PMOS	Base for 4x side bias mirror	3.2	9.6	2.1	2.1	7	7	0.313	3.57E-06	1.13E-07	0.152	1.137	0.971	0.24	

Pearl scaling spreadsheet: 0.5 micron process sizes derived from the MM9/Pearl chip

Pearl Section				Pearl (um)		Scaled (um)		Scaled (λ)		MOSFET Bias and SS Parameters							
Pearl RefDes	# in par.	Type	Function	L	W	L	W	L	W	ID (ua)	gm	gds	Vov	VGS	VTH	Test VDS	Cas-code FOM
M3	1	PMOS	Base cascode	3.2	9.6	1.8	2.1	6	7	1.25	8.37E-06	4.98E-08	0.274	1.36	1.086	1.39	175
	3	PMOS	2x Base cascode	3.2	17.6	1.8	3.6	6	12	2.5	1.68E-05	1.55E-07	0.279	1.341	1.06	0.8	114
	2	PMOS	4x Base cascode	3.2	32	1.8	6.6	6	22	5	3.31E-06	3.12E-07	0.282	1.329	1.05	0.8	113
								0	0								
M4	2	NMOS	Control mirror control source	4.8	10.4	4.8	5.4	16	18	5	3.27E-05	4.44E-07	0.335	1.063	0.727	0.45	
M5	2	NMOS	Control mirror cascodes	3.2	16	2.4		8	0	5						0.8	
M6	3	NMOS	Control for PCASC cascode generation mirrors	4.8	6.4	3.9	3	13	10	2.5	1.90E-05	2.06E-07	0.308	1.095	0.771	0.45	
M7	3	NMOS	Cascodes for PCASC cascode generation mirrors	3.2	8	2.4	4.2	8	14	2.5	3.22E-05	9.25E-08	0.203	1.107	0.903	1.1	361
	2	NMOS	Additional cascodes for NCASC cascode generation	n.a	n.a	2.4	4.2	8	14	2.5	3.22E-05	9.25E-08	0.203	1.107	0.903	1.1	361
M8	2	NMOS	Diode-connected NCASC generation	38.4	8	41	4.2	136	14	2.5			0.213	1.604	0.743	0.461	377
M9	2	NMOS	Start current injectors	40	3.2	18	0.9	60	3	2.5				3		3	
M10	1	NMOS	Startup inverter bottom	4	4.8	1.5	2.1	5	7	n.a.							
M11	1	PMOS	Startup inverter top	11.2	4.8	2.4	1.5	8	5	n.a.	switch at 1.06 for vdd=2.6 and 1.16 for Vdd=3.0						
M12	2	PMOS	Diode-connected PCASC generation	17.6	12.8	9.6	2.1	32	7	2.5	1.70E-05		0.278	1.343	1.068	0.412	167
M13	2	PMOS	Cascodes for PCASC	3.2	17.6	1.8	3.6	6	12	2.5	1.68E-05	1.55E-07	0.279	1.341	1.06	0.8	114